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Self-Turn-on Phenomenon of SiC MOSFETs by Fast Switching Operation

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Abstract. The effect of the contact resistance between the p-well and the source electrode of SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) on the self-turn-on phenomenon was investigated experimentally. It was found that the contact resistance significantly affects the self-turn-on in addition to the conventional self-turn-on owing to the parasitic capacitances. To simulate this phenomenon, a circuit model including the contact resistance, p-well sheet resistance, and p-well/n+ region diode was created, and the simulation results were compared with the measurement results. Consequently, by considering the contact resistance and the forward recovery effect in the diode characteristics, the gate-induced voltage was calculated, with the results close to those of the experiment. Thus, the influence of contact resistance and p-well/n+ diode effects are clearly very important when operating SiC MOSFETs at high switching speeds.

Introduction

Higher-switching-frequency operation of SiC metal-oxide-semiconductor field-effect-transistors (MOSFETs) would reduce the volume of such passive components as capacitors and inductances in power electronics systems to achieve higher power densities of the systems [1]. When such an operation is performed, the switching loss increases and the efficiency decreases. Increasing the switching speed and shortening the switching time at ON and OFF are effective for reducing the switching loss of SiC MOSFETs。.

However, the resulting sudden change in the drain-source voltage (dV_{ds}/dt) of the MOSFET causes a large induced voltage at the gate electrode ($V_{ind.}$) because of the gate-drain capacitance (C_{gd}). Consequently, a self-turn-on phenomenon may occur [2]. Furthermore in the case of SiC MOSFETs, self-turn-on phenomena that cannot be explained by C_{gd} have been reported [3].

Therefore, experiments on the temperature dependence of the self-turn-on phenomenon and the effect of the contact resistance between the p-well and the source electrode were conducted. A mechanism for the self-turn-on phenomenon is proposed as a result of investigating the device physics of SiC MOSFETs.

Experimental Setup

Figure 1 depicts the experimental configuration used to study the self-turn-on of SiC MOSFETs. The SiC MOSFET was placed in the lower arm and was kept off by applying a negative gate bias voltage (V_{bias}), which was lower than the threshold voltage of the MOSFET. A high voltage (V_{DS}) was applied to the drain source electrode of the lower arm MOSFET by turning on the MOSFET of the upper arm.

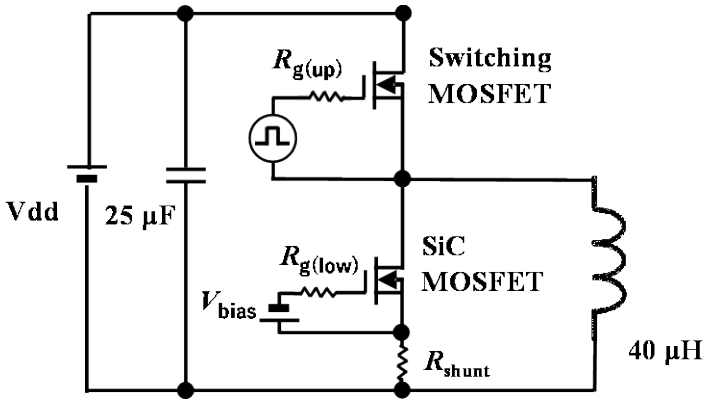

Fig. 1 Experimental configuration.

To control the applied dV_{ds}/dt of the lower arm MOSFET, the switching speed of the upper arm MOSFET was changed by the gate resistance ($R_{g\,(up)}$) of the upper arm.

To simplify the analysis of the voltage induced in the gate electrode and the self-turn-on phenomenon resulting from dV_{ds}/dt, the displacement current was prevented from flowing into the gate bias circuit. Therefore, the gate resistance ($R_{g(low)}$) was set to a value sufficiently larger than the impedance due to the input capacitance of the MOSFET.

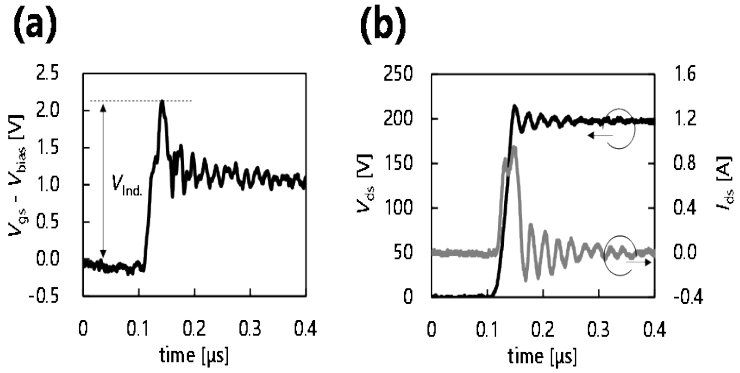

Fig. 2 Typical waveforms of (a) V_{gs}-V_{bias} and (b) V_{ds} and I_{ds}.

Figure 2 shows a typical waveform of a lower-arm SiC MOSFET. Figure 2(a) shows the gate source voltage V_{gs} minus the V_{bias} offset, and Figure 2(b) shows the V_{ds} and drain source currents (I_{ds}). As shown in Figs. 2(a) and (b), when V_{ds} increases, a gate voltage is induced and the displacement current flows.

The gate induced voltage ($V_{ind.}$) by dV_{ds}/dt is defined as the deviation between the peak value and the initial value of V_{gs}, as shown in Fig. 2(a).

Self-turn-on was detected as follows. First, the gate bias voltage was set so that self-turn-on did not occur, and then the current flowing through the lower arm was measured while gradually increasing the bias voltage. When this current increased, it was determined that self-turn-on had occurred. The bias voltage at that time was defined as the self-turn-on prevention voltage ($V_{prv.}$).

In this experiment, planar 4H-SiC MOSFETs with a rated voltage of 1200 V and chip size of 0.03 cm2 were adopted.

Results and Discussion

In this section, the experimental results and the models that explain the results are described.

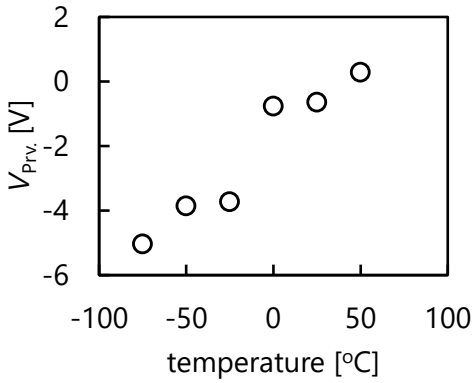

Fig. 3 Dependence of $V_{prv.}$ on measurement temperature at dV_{ds}/dt of approximately 20V/ns.

Figure 3 shows the relationship between the $V_{prv.}$ and measurement temperature. This experiment was performed under the condition of dV_{ds}/dt of approximately 20V/ns. As shown in Fig.3, the positive temperature dependence of $V_{prv.}$ was observed.

The traditional self-turn-on phenomenon is thought occur via C_{gd}. However, the temperature dependence of Cgd and Cgs is not strong enough to explain the temperature dependence of Vprv in Figure 3. The self-turn-on phenomenon in this experiment is clearly another phenomenon.

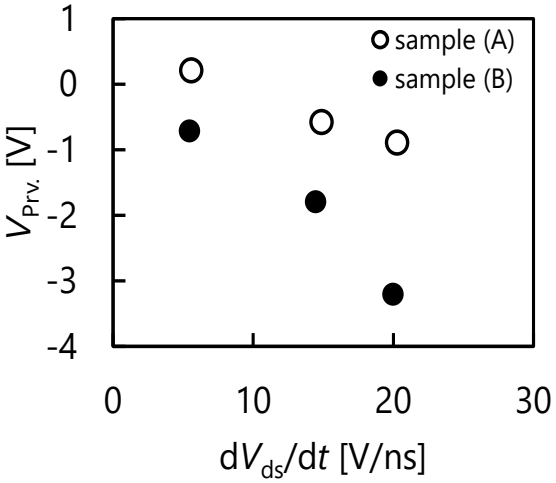

Fig. 4 Dependence of $V_{prv.}$ of samples (A) and (B) on dV_{ds}/dt at 25 degrees Celsius.

Figure 4 shows the dV_{ds}/dt dependency of $V_{prv.}$ using two samples. The experiments were conducted at 25 degrees Celsius. Sample A had a normal contact resistance (ρ_c) between the p-well and the source electrode, and sample B intentionally had a large ρ_c.

As shown in Fig. 4, the $V_{prv.}$ of sample B was lower than that of sample A. Moreover, the dependence of $V_{prv.}$ on dV_{ds}/dt was larger in sample B than in sample A. These experimental results show that the higher the contact resistance (ρ_c), the more likely the occurrence of the self-turn-on phenomenon.

It is well known that contact resistance increases as temperature decreases. Summarizing the results in Fig. 4, the phenomenon that $V_{prv.}$ has positive temperature dependence, as shown in Fig. 3, and it is considered to be caused by the temperature dependence of the contact resistance.

To understand the mechanism of the dependence $V_{prv.}$ on the temperature and contact resistance described in Figs. 3 and 4, the equivalent circuit model shown in Fig. 5 was developed. The model

included each capacitive component (C_{gs}, C_{gd}, and C_{ds}) of the MOSFET, the contact resistance ρ_c and sheet resistance (R_{sh}) of the p-well, including their temperature dependence [4], and the diode of the p-well and n+ region (p-well/n+ diode). In addition, the forward recovery characteristics was incorporated in the diode so that the transient characteristics could be simulated. The forward recovery characteristics were modeled by a series-connected variable resistor whose resistance changed according to the charge through the diode [5].

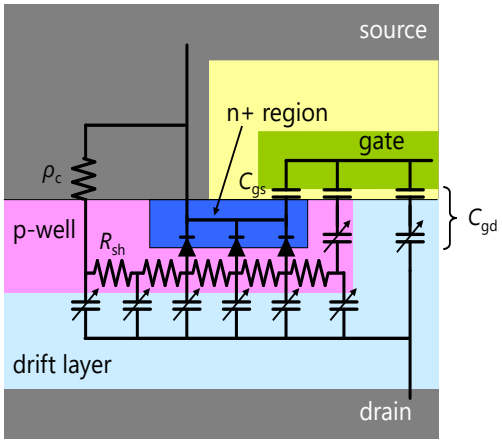

Fig. 5 Schematic of an equivalent circuit model.

In the simulation, the measured V_{ds} waveform was used as the drain voltage.

In the simulation, the experimental results of $V_{ind.}$ were compared with the simulation results. The simulation was performed using the three models: (I) a model that considered only C_{gs} , C_{ds} and C_{gd}, (II) a model that included all the components described in Fig. 5 except for the forward recovery characteristics of the p-well/n+ diode, and (III) a model that included the forward recovery effect in the p-well/n+ diode. The features of the model are summarized in Table I.

Table 1 Three types of models.

model	**Ⅰ**	**Ⅱ**	**Ⅲ**
C_{gs} & C_{gd}	✓	✓	✓
other capacitance	-	✓	✓
ρ_c & R_{sh}	-	✓	✓
p-well/n+ diode	-	✓	✓
forward recovery	-	-	✓

Table 2 Parameters for the simulation.

Parameters	Value
Contact Resistance	1mΩcm2
Sheet Resistance	20000Ω sq.
Cgs	48.8nF/cm2
Cds	$CJo = 24.4\left(\frac{nF}{cm2}\right), Vj = 3.5\,V, M = 0.56$
Cgd	$CJo = 9.2\left(\frac{nF}{cm2}\right), Vj = 1.0\,V, M = 0.8$

The parameters used in the simulation are listed in table 2. For Cds and Cgd, the drain voltage dependence was given by the following equation using the parameters in the table.

$$CJo \times (1 + \frac{Vds}{Vj})^{-M} \quad (1)$$

Figure 6 shows the dependence of the measured and calculated values of $V_{ind.}$ of sample A on (a) dV_{ds}/dt at 25 degrees Celsius and (b) temperature at dV_{ds}/dt of approximately 20V/ns.

Figure 6(a) shows the relationship between $V_{ind.}$ and dV_{ds}/dt. The red, blue, and white diamonds are the results of models I, II, and Ⅲ, respectively. The white circle represents the measurement results.

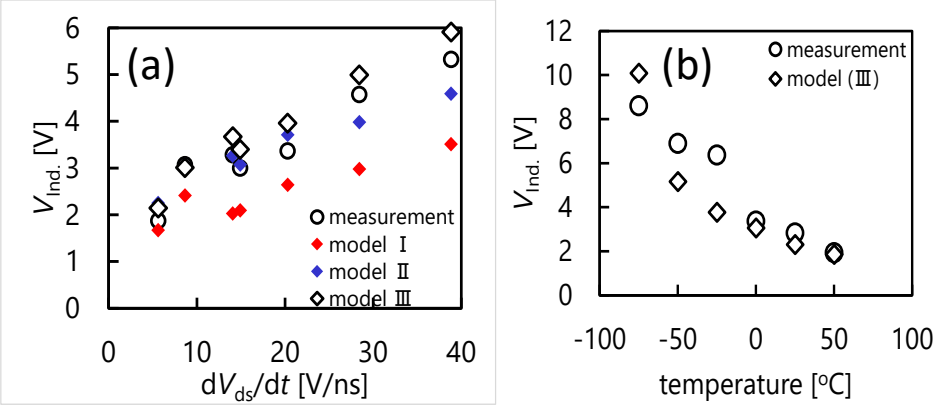

Fig. 6 Dependence of measured and calculated $V_{ind.}$ of sample A on (a) dV_{ds}/dt at 25 degrees Celsius and (b) temperature at dV_{ds}/dt of around 20V/ns.

As shown in Fig. 6(a), the calculated $V_{ind.}$ of model I shows a large deviation from the measured value and smaller dependence on dV_{ds}/dt. However, the results of model II show that $V_{ind.}$ is larger than that of model I and the difference from the measured value becomes small. This indicates that the potential fluctuation of the p-well caused by the displacement current flowing through the contact resistance and the sheet resistance affects $V_{ind.}$. However, if dV_{ds}/dt is large, the difference from the measured $V_{ind.}$ becomes large. This is because the induced voltage of the p-well is limited by the built-in potential of p-well/n+ diode in model II.

In model III, a transient high resistance was applied to the p-well/n+ diode to consider the forward recovery characteristics. Figure 6 shows that the $V_{ind.}$ values calculated using this model agreed well with the measured values, even at large dV_{ds}/dt values.

This indicates that the transient characteristics of the p-well/n+ diode are also important in the circuit analysis when the MOSFET is switched ON and OFF under the condition of a large dV_{ds}/dt.

Figure 6(b) shows the measured and calculated temperature dependences of $V_{Ind.}$. The dV_{ds}/dt at this time is approximately 20V/ns. As shown in the figure, the measured (white circles) and calculated (white diamonds) values agree well, confirming the validity of this model.

Summary

The SiC MOSFET self-turn-on phenomenon dependency on dV_{ds}/dt, temperature, and contact resistance was measured when dV_{ds}/dt was applied.

It was found that the self-turn-on prevention voltage ($V_{prv.}$) had a positive temperature dependence and was strongly influenced by contact resistance.

To simulate this phenomenon, a circuit model including contact resistance, p-well sheet resistance, and p-well/n+ region diodes was created and compared with the measured results. It was found that a closer calculation result to the experimental result could be obtained by considering the contact resistance and the forward recovery effect in the p-well/n+ region diode.

It was shown that the contact resistance and p-well/n+ diode characteristics are very important for the switching characteristics when SiC MOSFETs operate at a high switching speed.

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