Vertical-Type Amorphous-Silicon MOSFET IC's

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Abstract—**The performance of vertical-type amorphous-silicon (a-Si) MOSFET's has been improved significantly by employing native silicon dioxide as the gate insulator. The maximum field-effect mobility was 1.2 $cm^2/V \cdot s$. An E/E-type inverter and a seven-stage ring oscillator have been fabricated by integrating the vertical-type a-Si MOSFET. The minimum propagation delay time was 95 ns/stage. The characteristics of an *RS* flip-flop circuit are also described.**

I. Introduction

AMORPHOUS-SILICON field-effect transistors (a-Si FET's) have been investigated extensively for the application of large-area switching devices, such as matrix-addressed panel-displays [1] and contact-type image sensors [2]. The most serious problem of the present a-Si FET's is low operating speed due to low field-effect mobility of electrons in a-Si. Many researchers have demonstrated logic circuits by using the conventional FET structure [3]–[5], but their delay times were far from the required value for practical circuits. In order to attain a satisfactory speed, i.e., megahertz-rate operation, the transit time of electrons across the channel of a-Si FET's should be drastically decreased. A short channel would be an effective solution because the transit time is inversely proportional to the square of the channel length.

We have proposed a novel vertical-type a-Si FET [6], [7] whose channel length can be easily reduced to the submicrometer region since the channel is determined by the thickness of an intermediate insulator layer, and thus free from the photolithography limit. In this paper, we have described the improved performance of vertical-type a-Si FET's by incorporating the native silicon-dioxide gate and their circuit operation.

II. MOSFET Fabrication Process

Two major issues in fabricating high-performance vertical-type a-Si FET's are 1) excellent electrical properties at the insulator–a-Si interface, and 2) negligibly small parasitic capacitance and resistance. We have shown [7] that the second issue is satisfied by applying self-alignment technology and by employing highly conductive microcrystal-silicon (μc-Si) layers in the source and drain regions. The first issue has been successfully solved by applying a low-temperature thermal oxidation technique [8] to the vertical-type FET, as described in this paper.

Fabrication steps of the vertical-type a-Si MOSFET are similar to those reported in the previous work [7], that is, oxidation is achieved at 250°C pressurized nitric and sulfuric acid. In order to introduce the low-temperature thermal-oxidation method to the vertical-type a-Si FET process, however, we used a Cr/Ta double layer for the top (drain) electrode. The top Cr layer was chemically patterned and served only as the mask for reactive-ion etching to form an island. After the Cr layer was removed, the active n^- a-Si layer was deposited. Then the interface of the a-Si layer was oxidized by our low-temperature thermal-oxidation method. This is because the Cr layer was dissolved and the Ta layer was oxidized quickly in our low-temperature thermal-oxidation method.

A schematic cross-sectional view of the fabricated vertical-type a-Si MOSFET is shown in Fig. 1. The thicknesses of the upper Ta, $n^+\mu$c-Si, SiN, $n^+\mu$c-Si, and lower Ta layers were chosen as 200 nm, 300 nm, 1 μm, 300 nm, and 200 nm, respectively. The gate insulator is a double layer having 20- or 90-nm-thick CVD-SiO_2 and a 10-nm-thick native silicon dioxide. Mo and Al double layers 500 nm and 1 μm thick, respectively, were used for gate electrodes and interconnection lines.

The thickness of the active layer was determined as follows. When the active layer is thick, the drain current I_D is crowded under low drain voltages V_D and increases rapidly when V_D is more than a drain offset voltage V_{OFF}. The experimentally obtained relative value of V_{OFF} is shown in Fig. 2 as a function of the active layer thickness. V_{OFF} was decreased with decreasing the thickness. The thickness dependence of field-effect mobility μ_{FE} under low V_D conditions is also shown in Fig. 2. The mobility, however, began to decrease abruptly when the active layer was decreased below 50 nm. Thus we have concluded that the optimum active layer thickness in the vertical-type FET is about 80 nm.

III. Transistor Performance

Typical FET characteristics are shown in Fig. 3. The drain current I_D started to increase linearly with V_D from $V_D \simeq 0$ and showed clear saturation characteristics since parasitic resistances in the source and drain are very low. The threshold voltage was about 3 V. The field-effect mobility under low V_D conditions was 0.43 $cm^2/V \cdot s$. The characteristics were changed slightly even when the source and drain were exchanged. It should be noted that the

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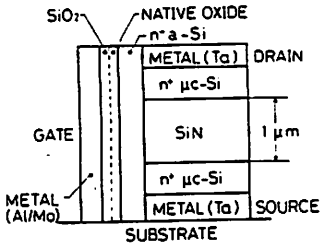

Fig. 1. Cross-sectional view of the vertical-type a-Si MOSFET.

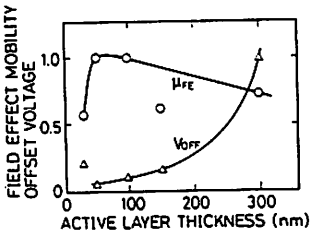

Fig. 2. Active layer thickness versus offset voltage V_{OFF} and field-effect mobility μ_{FE} in the vertical-type a-Si MOSFET.

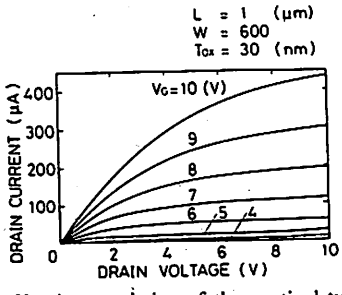

Fig. 3. Linear I_D-V_D characteristics of the vertical-type a-Si MOSFET. The channel length and width were 1 and 600 μm, respectively. The total gate oxide thickness was 30 nm. The active a-Si layer thickness was 80 nm.

field-effect mobility of the FET with only a 10-nm-thick native silicon-dioxide gate was as high as 1.2 $cm^2/V \cdot s$ when $V_D = 0.1$ V and $V_G = 1.5$ V. Fig. 4 shows I_D-V_G characteristics. A large on/off current-ratio was obtained under low V_D conditions. The ratio, however, decreased rapidly with increasing V_D due to the rapid increase in the off current. There were large variations in the off current values among devices, but even the best on/off ratio was still less than 10^2 at $V_D = 10$ V. This value is inferior to that necessary for matrix-addressed panel displays [9] and also for high-speed dynamic circuits [10].

There are three possible origins of the large leakage current under high V_D conditions. They are: 1) hole conduction, i.e., p-channel operation along the front SiO_2-a-Si interface; 2) space charge-limited current (SCLC) flowing in the bulk of the a-Si layer; and 3) electron conduction along the back a-Si–SiN interface, induced by the back-gate effect of the drain through a thick intermediate SiN layer. Since I_D did not increase sharply at negative V_G, the possibility of hole conduction is excluded. A separate experiment using an n-i-n sandwich structure with a 1 μm-thick n^- layer indicated that the SCLC density was less than 2 A/cm^2 at 10-V bias voltage while the average current density flowing in the active region of the FET biased at $V_G = 0$ and $V_D = 10$ V was more than 15 A/cm^2.

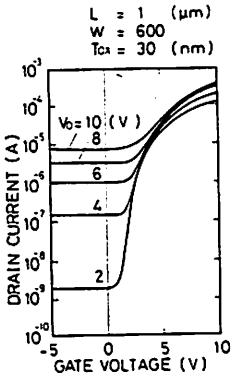

Fig. 4. Semi-logarithmic I_D-V_G characteristics of the vertical-type a-Si MOSFET. The channel length and width were 1 and 600 μm, respectively. The total gate oxide thickness was 30 nm. The active a-Si layer thickness was 80 nm.

Thus, the SCLC cannot account for the observed large leakage current. Therefore, we have concluded that the back-gate effect is the most important for large leakage current. This conclusion is consistent with the large variation of the off-current value since the back a-Si–SiN interface characteristics are difficult to control.

IV. Integrated Circuit Performance

An integrated E/E inverter circuit has been evaluated. The channel widths of the driver and load were 600 and 60 μm, respectively. The channel length was 1 μm. Transfer curves for various gate voltages V_{GG} of the load FET are shown in Fig. 5. The drain voltage V_{DD} of the load transistor was fixed at 10 V. The total gate oxide thickness was 30 nm. The active n^- a-Si layer was 80 nm. Logical "NOT" operation was obtained clearly. The maximum small-signal gain was 2.4 at $V_{GG} = 15$ V.

A microscopic photograph of the seven-stage ring oscillator integrated using seven similar inverters is shown in Fig. 6. There is an on-chip FET detector at the left of the picture. The long and narrow white stripes are not of the channel region but of the 20-μm-wide top Ta layer. The channel is formed at the sidewall of the stripe.

The power dissipation per gate is shown as a function of the propagation delay time in Fig. 7. The circles and triangles in the figure designate results from FET's with 20- and 90-nm-thick CVD-SiO_2 layers, respectively, deposited on a 10-nm-thick native silicon dioxide. The active n^- a-Si layer was 80 nm. A minimum propagation delay time of 95 ns/stage was obtained at $V_{DD} = 20$ V and $V_{GG} = 50$ V. This value is about one-half of the best value reported to date [5]. But, this delay is still five times longer than the value calculated by using the measured value of the mobility at 0.5 $cm^2/V \cdot s$ at V_{DD} of 20 V and for a total capacitance of 0.4 pF. The power delay products were 120 and 170 pJ for FET's with 20- and 90-nm-thick CVD-SiO_2 layers.

The RS flip-flop with a NOR configuration was also evaluated by using FET's with a 20-nm-thick CVD-SiO_2 layer. The active n^- a-Si layer was 80 nm. Reset and set signals of nonoverlapping 10-V clock pulses were applied to the driver FET gates. V_{DD} was kept at 10 V and V_{GG} =

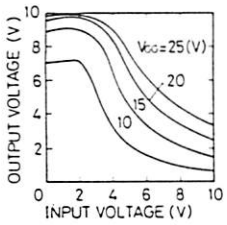

Fig. 5. The transfer characteristics of the E/E-type inverter formed by a vertical-type a-Si MOSFET.

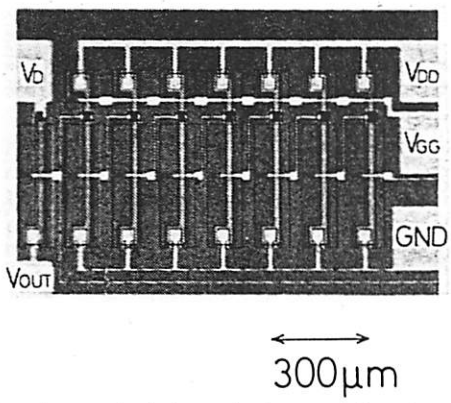

Fig. 6. The microscopic photograph of a seven-stage ring oscillator.

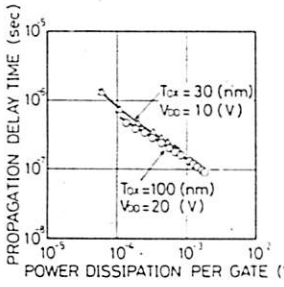

Fig. 7. Relation between power dissipation per gate and propagation delay time of seven-stage ring oscillator.

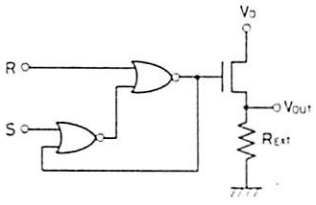

Fig. 8. Measuring circuit of dynamic response of *RS* flip-flop. Output voltage V_{OUT} was detected by on-chip source follower circuit connected at the NOR gate with *R* input. External resistance R_{EXT} was 5 kΩ. Drain voltage of on-chip FET was 0.2 V.

25 V. Output responses were detected by an on-chip FET detector connected at the NOR gate with *R* input. The circuits measuring for the dynamic response of *RS* flip-flop are shown in Fig. 8. The output waveforms are shown in Fig. 9. The clock frequency was 100 kHz. Sharp impulses at the rising and falling edges of the *S* and *R* pulses were due to capacitive coupling in the measurement system. The rise time of the output voltage was longer than its fall time because two inverters should change their states for the set signal. We evaluated the rise time by subtracting the capacitive coupling waveform at $V_{GG} = 0$, and it was

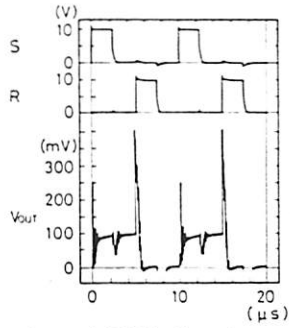

Fig. 9. Response waveform of *RS* flip-flop. Output voltage V_{OUT} was detected by on-chip source follower circuit connected at the NOR gate with *R* input.

about 330 ns. This value agreed well with the delay time estimated by the ring oscillator experiment. Thus, we expect that, by eliminating capacitive coupling in the measuring apparatus, 1-MHz operation will be possible with the present devices.

V. Conclusion

The electrical properties of vertical-type a-Si MOSFET IC's have been improved by employing native silicon dioxide as a gate insulator. A minimum propagation delay time of 95 ns/stage has been achieved by a prototype ring oscillator. The flip-flop circuit is estimated to operate at 1 MHz. Superior circuit performance will be attained by further optimizing the device structure and circuit configuration.

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