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High-Mobility Amorphous-Silicon MOS Transistors

Hiroyuki OKADA, Yasutaka UCHIDA and Masakiyo MATSUMURA

Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Meguro-ku, Tokyo 152

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Process conditions for gate oxide formation in amorphous-silicon MOS transistors have been investigated systematically. It was found that the n^+ micro-crystal silicon layer just above the active transistor region should be removed before the gate oxidation at 250°C. Annealings in nitrogen ambient just after the oxidation and in hydrogen ambient after gate electrode evaporation were also effective. The highest field-effect mobility measured by the transistor fabricated under the optimum process conditions was about 4.8 cm^2/Vs. Dynamic response characteristics have also been evaluated.

§1. Introduction

Amorphous-silicon field-effect transistors (a-Si FETs) have been investigated extensively for the purpose of applying them to large-area switching elements for flat-panel displays[1-4] and image sensors.[5,6] Conventional a-Si FET with deposited silicon-nitride (SiN) layer as a gate insulator, however, has various problems: (1) the FET is not sufficiently stable, (2) fabrication process for the FET with small parasitic elements is very complicated and (3) the electrical characteristics of the FET are not satisfactory. These problems are mainly caused by the constraint of the three layers of SiN, active a-Si and n^+a-Si being deposited within one vacuum-pumpdown, and by the inferior bulk and interface characteristics of SiN.

We have proposed a new low-temperature thermal-oxidation method of silicon[7] and applied it to a-Si MOSFET process.[8] Since the silicon-dioxide (SiO_2)/a-Si interface is formed inside the original a-Si layer and SiO_2 has a wider band gap than SiN, this SiO_2/a-Si system has potentially superior electrical properties than the SiN/a-Si system.[9] Preliminary results[8] indicated that the a-Si MOSFET with the native SiO_2 gate has promising electrical performance, such as, good long-term stability and sufficiently small parasitic capacitance and resistance; it can also be fabricated by 4 photomasks. The most serious drawback of this a-Si MOSFET process is the necessary application of high pressure during the oxidation. However, we have also reported[10] that there is a way to eliminate the high pressure during the oxidation. Thus, we hope that the a-Si MOSFET can solve the abovementioned serious problems in the present a-Si FET.

In this paper, we intend to verify the superior SiO_2/a-Si interface properties by clarifying the optimum conditions for forming a good a-Si MOS structure and by presenting the superior static and dynamic performances of the a-Si MOSFET.

§2. Experimental results

A cross-sectional view of the planar a-Si MOSFET is shown in Fig. 1. The basic structure and fabrication process are the same as those reported in a previous letter.[8] The most important features of this planar a-Si MOS transistor are its superior insulator/semiconductor interface properties as a result of use of the SiO_2 layer thermally grown inside the original a-Si layer. This allows stable and high mobility operation of the a-Si MOSFET. However, experimental confirmation of the high mobility operation has not yet been achieved due to lack of optimal process conditions. Here, we have compared FET

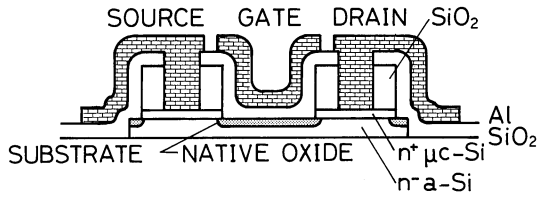

Fig. 1. Cross-sectional view of planar a-Si MOS transistor.

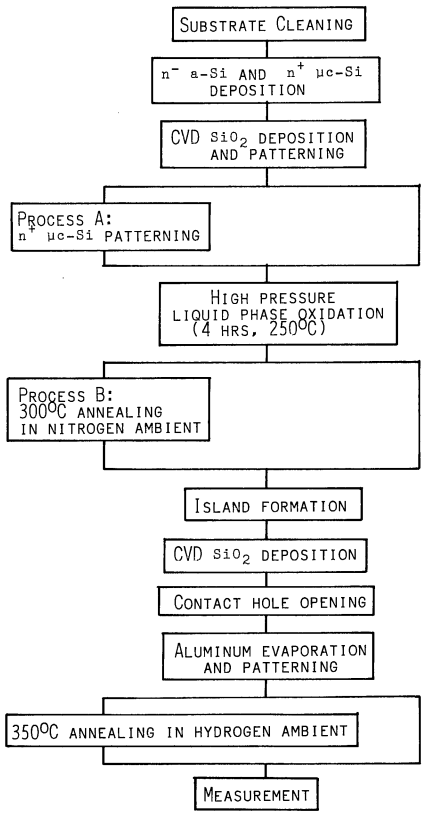

Fig. 2. Process flow of a-Si MOSFET under study.

characteristics fabricated by various process conditions and optimized fabrication conditions.

Process steps studied are summarized in Fig. 2. First, undoped n^-a-Si (300–450 nm thick) and P-doped n^+ microcrystal silicon (μc-Si) (less than 20 nm in thickness) layer were deposited on a thermally oxidized single-crystal silicon surface. The 500 nm-thick CVD SiO_2 layer was then deposited at 300°C and was etched off except for source and drain regions. The $n^+\mu$c-Si layer was either etched off (process A) or not (process $\bar{A}$). Then, samples were encapsulated in a quartz ampoule with a mixture of nitric and sulfuric acids and heated to 250°C for 4 hours. The oxide layer grown inside the n^-a-Si layer was 12 nm thick but the layer inside the $n^+\mu$c-Si layer was 17 nm thick. Samples were then either annealed in nitrogen ambient for 30 minutes (process B) or not (process $\bar{B}$). Next, all layers outside the transistor portion were etched off and the 140–160 nm thick CVD SiO_2 layer was deposited again at 300°C to increase the gate oxide thickness. Contact holes were opened and aluminum was evaporated and patterned. Finally, samples were either annealed or not in hydrogen ambient at 350°C for 30 minutes.

Table I shows typical characteristics in (1) field-effect mobility (μ_{FE}) calculated from drain current (I_D)—drain voltage (V_D) characteristic under low V_D conditions, (2) subthreshold slope ($S=\partial V_G/\partial \log I_D$, where V_G is the gate voltage) and (3) on-off current ratio ($R=\log(I_{ON}/I_{OFF})$) of FETs formed by various fabrication conditions. I_{ON} and I_{OFF} were defined as the maximum and minimum current over an all gate voltage swing within a gate insulator breakdown. The channel length (L) and width (W) were 20 μm and 960 μm, respectively. For the FET formed by process A, μ_{FE} and $\log(I_{ON}/I_{OFF})$ were larger and S was smaller than those, respectively, formed by process $\bar{A}$. Thus, it was concluded that removing the $n^+\mu$c-Si layer before the oxidation is effective in improving FET performance. For the FET formed by process B, all three values were improved in comparison with those formed by process $\bar{B}$, and remarkable improvements in FET characteristics were also obtained by hydrogen annealing. From these results, it is concluded that processes A, B and hydrogen annealing are useful.

Values of S and R for the optimized a-Si MOSFET are about the same as the typical values of conventional a-Si FET. However, for S value, the difference in dielectric constants between SiO_2 and SiN must be taken into account. For R value, p-channel operation causes the minimum drain current in the a-Si MOSFET, while conventional a-Si FET usually does not show the p-channel operation. This peculiar feature is attributed to the effect of large interface state density below the midgap of a-Si in the SiN/a-Si system. Thus existence of the p-channel operation in the a-Si MOSFET is further evidence of the good interface properties. The p-channel operation, however, should be eliminated from an application point of view. This should be achieved by an improvement of blocking characteristics of the $n^+\mu$c-Si layer, but not by an application of inferior interface properties.

Figure 3 shows the I_D-V_G characteristics of the FET with the highest mobility. The gate capacitance (C_{OX}) was 2.2×10^{-8} F/cm^2. V_D was kept at 10 V. On-current and off-current were 270 μA and 10^{-10} A, respectively. Subthreshold slope was 1.2 V/decade. Threshold voltage V_T

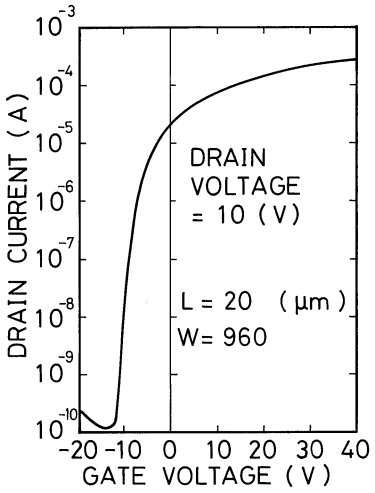

Fig. 3. Semi-logarithmic I_D-V_G characteristics of the a-Si MOSFET with the highest mobility.

Table I. Typical values of μ_{FE}, S and R for a-Si MOSFETs formed by various fabrication conditions.

·Effects of process A and B

(1) Field Effect Mobility μ_{FE} [cm^2/Vs]

	Process B	Process $\bar{B}$
Process A	2.0	1.3
Process $\bar{A}$	1.3	0.44

(2) Subhreshold Slope S [V/decade]

	Process B	Process $\bar{B}$
Process A	2.5	3.5
Process $\bar{A}$	3.3	9.1

(3) On-Off Current Ratio R

	Process B	Process $\bar{B}$
Process A	4.3	4.2
Process $\bar{A}$	4.0	3.6

·Effects of hydrogen annealing

		Before Annealing	After Annealing
Field Effect Mobility μ_{FE}	[cm^2/Vs]	2.0	2.7
Subthreshold Slope S	[V/decade]	2.5	1.2
On-Off Current Ratio R		4.3	6.3

was 9 V and field-effect mobility was 2.7 cm^2/Vs. However, the drain current was still high at $V_G=0$ V and negative V_G of about -10 V should be applied for sufficiently small current. This problem was solved by slightly etching the n^-a-Si layer before oxidation.

It was found that parasitic resistance still decreased the mobility in this high μ_{FE}FET. Thus, long channel FET was made in a similar manner and evaluated for the purpose of eliminating the parasitic resistance effect. Both L and W were 200 μm. Gate capacitance was 2.5×10^{-8} F/cm^2. I_D-V_D characteristics are shown in Fig. 4. V_T was rather high (about 25 V).

From the FET characteristics shown in Fig. 4, μ_{FE} under low V_D was calculated by using the single crystal MOSFET theory as,

$$\mu_{FE}=(L/W)(1/C_{OX})(\partial/\partial V_D)(\partial I_D/\partial V_G). \quad (1)$$

$\mu_{FE}-V_G$ characteristics are shown in Fig. 5. V_D was 6 V. μ_{FE} increased rapidly when V_G was increased from V_T and decreased gradually when V_G was much higher than V_T. The maximum μ_{FE} value under low V_D conditions was as high as 4.8 cm^2/Vs.

Dynamic current response has been measured by using circuits as shown in Fig. 6(a) and (b). L and W were 5 and 200 μm, respectively, and the maximum μ_{FE} value of the FET under study was 1.0 cm^2/Vs. External resistance R was 1 kΩ. The output terminal V_{OUT} was connected to a probe having a capacitance of 11pF. In Fig. 6(a), dc drain voltage was kept at 50 V or 0 V, while 50 V voltage pulse of 1/10 duty was applied to the gate, and in (b), dc source voltage was kept at 0 V or -50 V while -50 V voltage pulse of 1/10 duty was applied to the gate. There were no obvious differences in output current waveforms in (a) and (b). Output voltage response of the circuit shown in Fig. 6(a) is shown in Fig. 7. Zigzag patterns in the waveforms were caused by LC resonance of measuring system and there was slight gate-source and gate-drain capacitive coupling. By subtracting the waveform for $V_D=0$ V from that for $V_D=50$ V, the transistor current waveform was evaluated as shown by the lower trace in Fig. 7. Simple subtraction will generate an error, especially in turn-off characteristics because the initial condition for discharging is changed by the transistor current. However, in the case of Fig. 6(a), since direction of the transistor current is the same as that of the discharging current, simple subtraction does not result in underestimation of turn-off time. Turn-on time t_r was

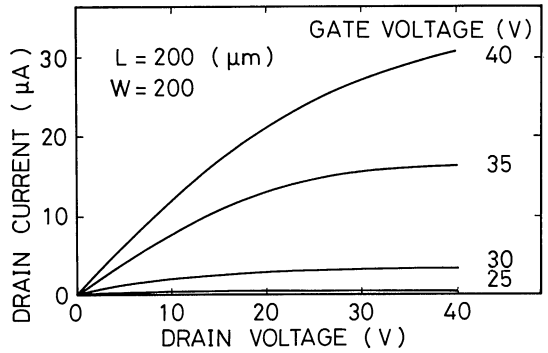

Fig. 4. Linear I_D-V_D characteristics of the long channel a-Si MOSFET.

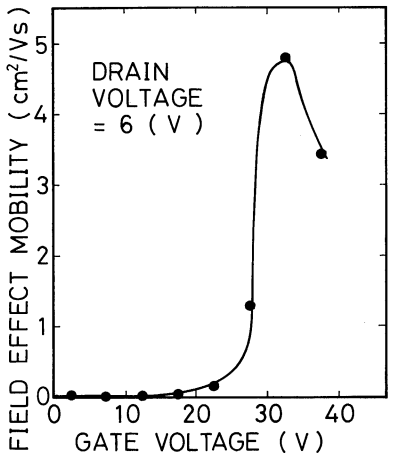

Fig. 5. $\mu_{FE}-V_G$ characteristics calculated from the long-channel a-Si MOSFET characteristics shown in Fig. 4.

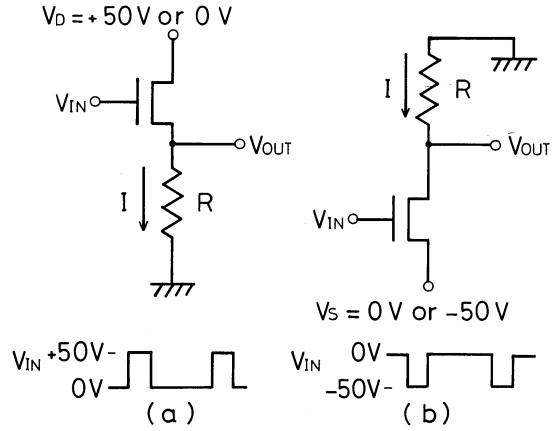

Fig. 6. Measuring circuit of dynamic response of the a-Si MOSFET.

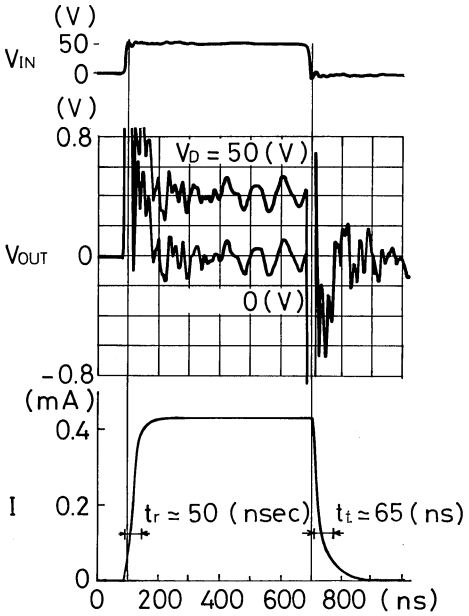

Fig. 7. Output voltage waveforms (upper trace) of a-Si MOSFET driven by the circuit shown in Fig. 6(a) and current waveform (lower trace) evaluated from voltage waveforms. Dc drain voltage was alternated between 0 V and 50 V. The output terminal V_{OUT} was connected to a probe having a capacitance of 11pF.

about 50 ns and turn-off time t_f was about 65 ns. Response time of external measuring circuit by the effect of probe capacitance and R was about 25 ns and 9 ns, respectively. These rise and fall times were determined by the external circuit parameter. If we assume that these values can be subtracted from turn-on and turn-off characteristics, the intrinsic t_r and t_f were less than 14 ns and 31 ns, respectively. Since these values were not so different from 2.3 times transit time (=5 ns) of electrons, localized states seem not to cause serious problems in dynamic response.[11)]

§3. Conclusion

Effect of detailed conditions for the gate oxide formation in a-Si MOSFETs have been investigated and the optimum conditions clarified. The maximum field-effect mobility measured was 4.8 cm^2/Vs under low drain voltage conditions. Superior dynamic performance of a-Si MOSFET has been also demonstrated. Turn-on and turn-off times reached 14 ns and 31 ns, respectively. These results indicate that inferior FET performances reported to date arise mainly from inferior interface properties of the SiN/a-Si system. However, there still remains the serious problem in the present oxidation method that the grown oxide is not sufficiently thick. Better performances will be obtained by further improving the oxidation method.

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