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Organic heterojunction transistors for mechanically flexible multivalued logic circuits

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Organic multivalued logic circuits (OMVLs) have drawn tremendous attention due to their high data processability and simple fabrication techniques. However, OMVLs have so far been achieved only on rigid silicon substrates, and this limits their potential for broader applications. In this study, we develop an organic ternary inverter on plastic substrates. The inverters showed well-balanced ternary logic states with high voltage gain and low power consumption. Importantly, the devices exhibited stable operation even after 100 bending cycles, demonstrating high flexibility and reliability. This device has high potential to attain mechanical flexibility and data handling capability at the same time.

Supplementary material for this article is available online

Flexible, stretchable and lightweight electronic devices such as thin-film transistors, logic gates and integrated circuits (ICs) have received enormous attention due to their potential applications in the internet-of-things (IoT) and wearable electronics.[1–5] Apart from their application to bendable flat panel displays, wearable and ultrathin ICs can also be used in the form of stickers as identification tags and in healthcare applications to monitor essential body parameters.[6,7] Organic semiconductors play a pioneering role in advanced electronic applications such as this, not only due to their superior electrical and optical properties but also because of their intrinsic mechanical flexibility that enables the development of circuitry on practically any kind of common surface such as paper, plastics and fabrics.[8–12] However, the chief limitation of organic electronics, i.e. low data processability, should be noted. This is because modern lithographic technologies cannot be applied to organic semiconductors. Multivalued logic circuits (MVLs) predominate in this regard, because they can exhibit three or more logical states, and thus can handle higher volumes of information than conventional binary logic circuits.[13–20] Additionally, MVLs can drastically minimize chip area by reducing the number of constituent devices and enable the development of densely ICs.[21–23] OMVLs are a potential game changer for next-generation IoT electronics, as they can achieve both high integration density and mechanical flexibility together with the advantage of easy patterning processes and low production costs. Several attempts have recently been made to develop high-performance OMVLs.[24–26] In these studies, pn-heterojunctions played an important role in realizing ternary logic states. However, all were implemented on flat and rigid silicon substrates, which limits their range of potential applications. Flexible MVLs, therefore, need to be developed to be able to fully exploit the advantages of organic semiconductors and to further expand the low-power, wearable electronic application prospects of these ICs.

In this study, we tackled this key challenge by developing a flexible organic ternary logic circuit. The logic circuit is constructed by combining an n-type transistor and a heterojunction transistor (HT) that consists of two organic semiconductors: PhC_2H_4-benzo[de]isoquinolino[1,8-gh]quinolone diimide (PhC2-BQQDI) and 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT) as n-type and p-type semiconductors, respectively.[27,28] Other key materials are insulating films that act as gate dielectric layers. One is poly (methyl methacrylate) (PMMA), which is used to prioritize mechanical flexibility. The other is hafnium oxide (HfO_2), which is employed specifically for low-voltage operation owing to its high dielectric constant. The inverters with both dielectric layers exhibit well-balanced ternary logic states, full-swing operation and high gain values. Most importantly, the inverters operated steadily after several cycles of repeated substrate bending, showing considerable potential for use in wearable electronic applications.

Figure 1(a) shows a schematic illustration of the ternary inverter with the PMMA dielectric layer, a top view photograph and the molecular structures of PhC2-BQQDI and C8-BTBT. The pn-heterojunction (C8-BTBT/PhC2-BQQDI) is formed between the V_{DD}–V_{OUT} electrodes. This part is therefore termed an HT. Meanwhile, the difference in V_{GND} and V_{OUT} provides the drain bias voltage for operating the n-type (PhC2-BQQDI) transistor. The device dimensions (width and lengths of the channels) are indicated in the photograph. The ternary inverter was implemented by combining the HT in series connection with a PhC2-BQQDI transistor on the flexible polyethylene naphthalate (PEN: DuPont Teijin, Teonex®) substrates. First, a 200 nm thick PMMA layer was spin-coated on the PEN substrates to reduce the surface roughness. Next, Cr (4 nm)/Au (30 nm) bilayer electrodes were thermally evaporated to form the gate electrodes. On top of the gate electrodes, another PMMA (300 nm) layer was spin-coated to serve as the gate dielectric layer. Then, organic semiconducting layers, PhC2-BQQDI (≈16 nm) and C8-BTBT (≈19 nm), were thermally evaporated at a background pressure of 10^{-7} Pa onto the PMMA surface as n-type and p-type channels,

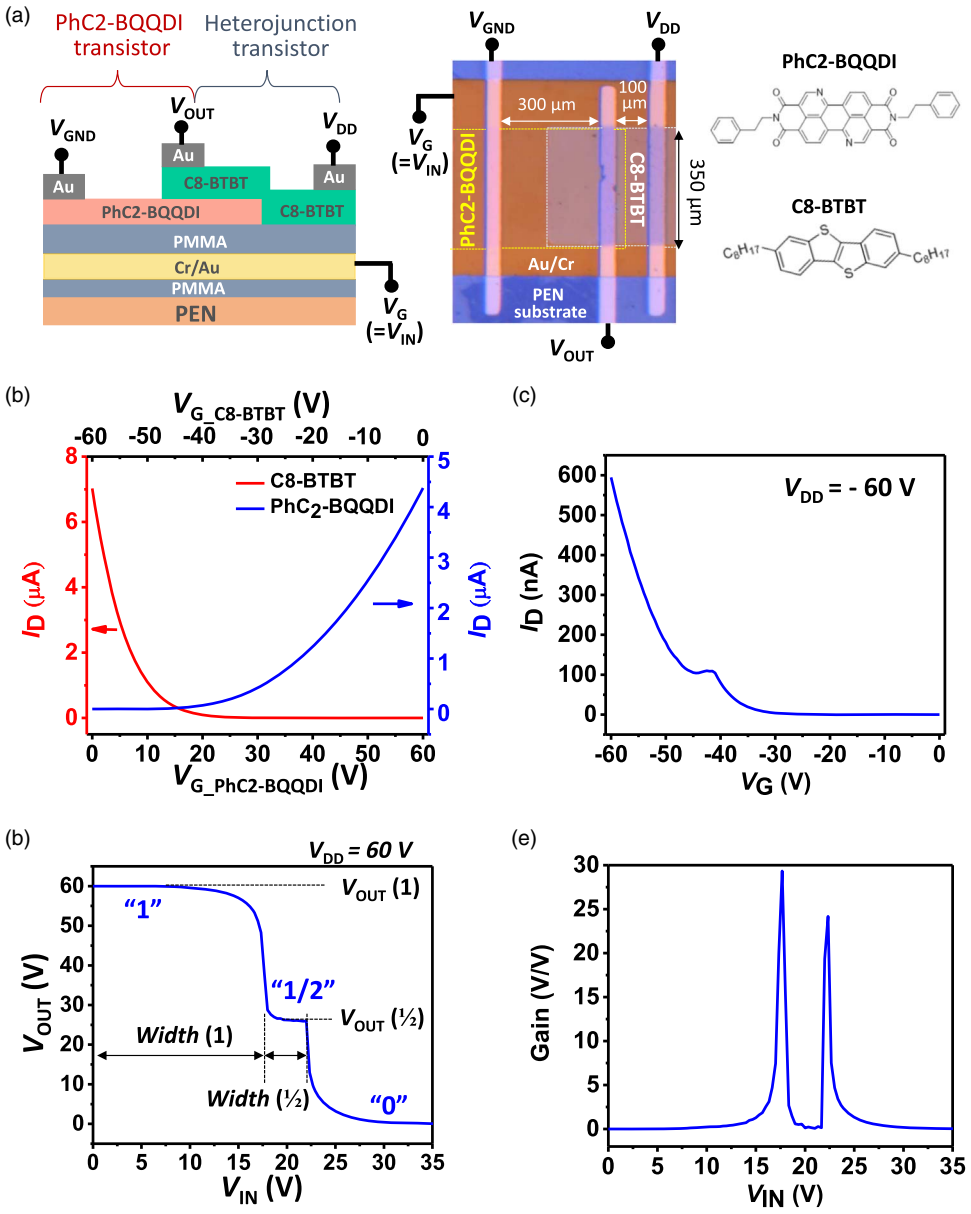

Fig. 1. (Color online) (a) Schematic illustration of the ternary inverter comprising the heterojunction transistor and the n-type PhC2-BQQDI transistor, top view photograph showing the device dimensions and chemical structures of PhC2-BQQDI and C8-BTBT. (b) Transfer characteristics at V_D = |60| V of the C8-BTBT (red line) and PhC2-BQQDI (blue line) transistors. (c) Transfer characteristics of the heterojunction transistor at V_{DD} = –60 V. (d) Voltage transfer characteristics of the ternary inverter at V_{DD} = 60 V. Parameters that define the device performance (V_{OUT} levels and V_{IN} widths) are also shown. (e) Gain profile of the inverters as a function of V_{IN}.

respectively, using corresponding shadow masks. These two channel layers were partially overlapped to form the heterojunction, which plays the most crucial role in yielding negative differential transconductance (NDT). Next, gold films, comprising the source and drain electrodes, were thermally evaporated using another shadow mask to complete the HT configuration. Finally, an additional electrode, namely, an output electrode, was simultaneously formed between the source and drain electrodes to monitor the output voltage (V_{OUT}). Here, it should be noted that the C8-BTBT layer in the HT was connected from the source to the drain electrodes to obtain a high on-current at high V_G region, as described by Kim et al.[25)]

Figure 1(b) shows the transfer curves of the C8-BTBT and PhC2-BQQDI transistors. These were measured individually by a semiconductor parameter analyzer (Agilent, B1500A), separately from the HT, to examine the fundamental properties of the respective channels. The output curves are also shown in Fig. S1 in the supporting information for reference (available online at stacks.iop.org/APEX/14/081004/mmedia). All measurements were carried out at room temperature in an ambient atmosphere, in dark conditions. Under these conditions, stable and repeatable operations were confirmed for both p- and n-type transistors. The PhC2-BQQDI transistor (blue line) showed an on/off ratio of approx. 10^6 along with an electron mobility of 0.2 ± 0.07 cm^2 V s^{-1}. On the other hand, the C8-BTBT transistor (red line) showed an even higher on/off ratio of approx. 10^8 and a hole mobility of 1.2 ± 0.2 cm^2 V s^{-1}. The threshold voltages (V_{th}) of the respective transistors were 18 and −44 V.

These high carrier mobilities were also replicated in the performance of the HT, as shown in the transfer characteristics in Fig. 1(c). Here, a bias voltage (V_{DD}) of –60 V was applied to the drain electrode, and the source electrode was

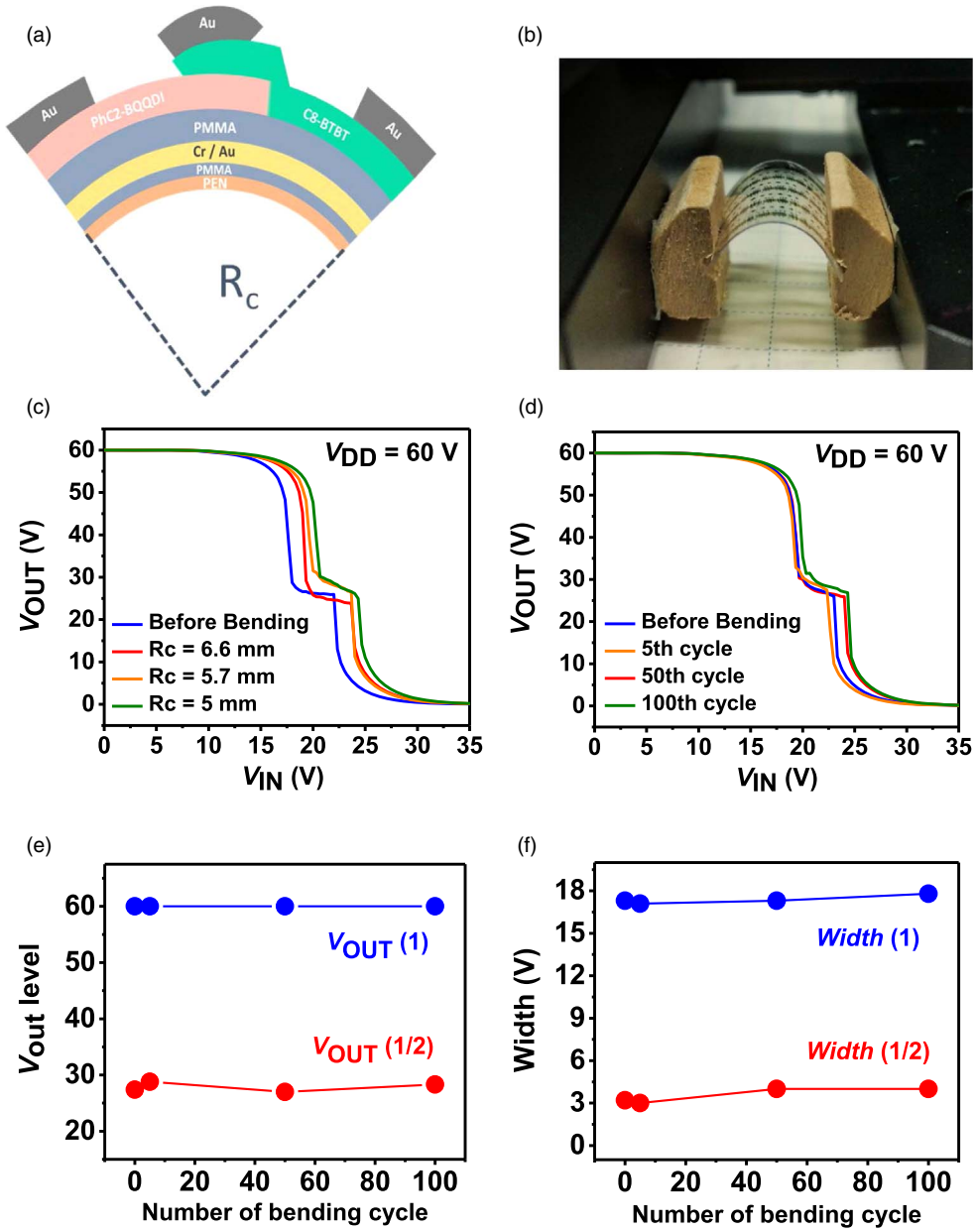

Fig. 2. (Color online) (a) Schematic illustration of the bent device structure; R_c represents the bending radius (b) Photograph of the setup for bending test (c) voltage transfer characteristics (VTCs) of the inverters as a function of bending radii (d) VTCs as a function of bending cycles at $R_c = 5$ mm (e) Variations of logic state output voltage levels and (f) logic state widths as a function of bending cycle. [Before Bending -> Before bending; Number of bending cycle -> Number of bending cycles.]

grounded (V_{GND}). The gate voltage (V_G) was provided to the bottom gate electrode. Due to the favorable transport of electrons and holes across the junction, the HTs exhibited a high peak current (I_{peak}) of 100 nA at a gate voltage (V_{peak}) of −41 V followed by the NDT up to $V_G = -44.5$ V. At higher V_G ranges, the continuous C8-BTBT layer resulted in a high on-current (I_{on}) of 600 nA at $V_G = -60$ V. As a result, an on/off ratio of approx. 10^6 was yielded at an off-current (I_{off}) of 0.3 pA at $V_G = -6$ V.

The NDT characteristics and high on/off ratio thus obtained in the HTs enabled us to operate the ternary inverter as shown in Fig. 1(d). The logic circuit showed a complete V_{OUT} modulation from V_{DD} (60 V) to ground voltage (0 V), yielding three distinct and well-balanced logical states: logic 1 at V_{OUT} (1) = V_{DD} = 60 V, logic ½ at V_{OUT} (½) = 26 V (≈V_{DD}/2) and logic 0 at V_{OUT} = ground. Here, the V_{OUT} (½) level is determined mainly by the balance of the respective channel resistances. The I_D and channel lengths are the key parameters. The value of I_D as a function of V_{IN} is shown in Fig. S2. Another important benefit of the inverter is the high DC voltage gain values shown in Fig. 1(e). The inverter was able to yield gain values as high as 29.5 V/V and 24 V/V at the first (logic 1 to logic ½ transition point) and second transition (logic ½ to logic 0 transition point) points, respectively. These are higher than for most previously reported ternary logic circuits.[14,18,25)]

Next, we carried out cyclic bending tests to evaluate the mechanical flexibility and reliability of the ternary inverters. The bending direction is schematically illustrated in Fig. 2(a), where R_c represents the bending radius of the curvature. Figure 2(b) shows a photograph of the setup under bent conditions. First, the electrical characteristics of the devices were measured as a function of the bending radii. All the data were obtained in the flat form after the bending tests.

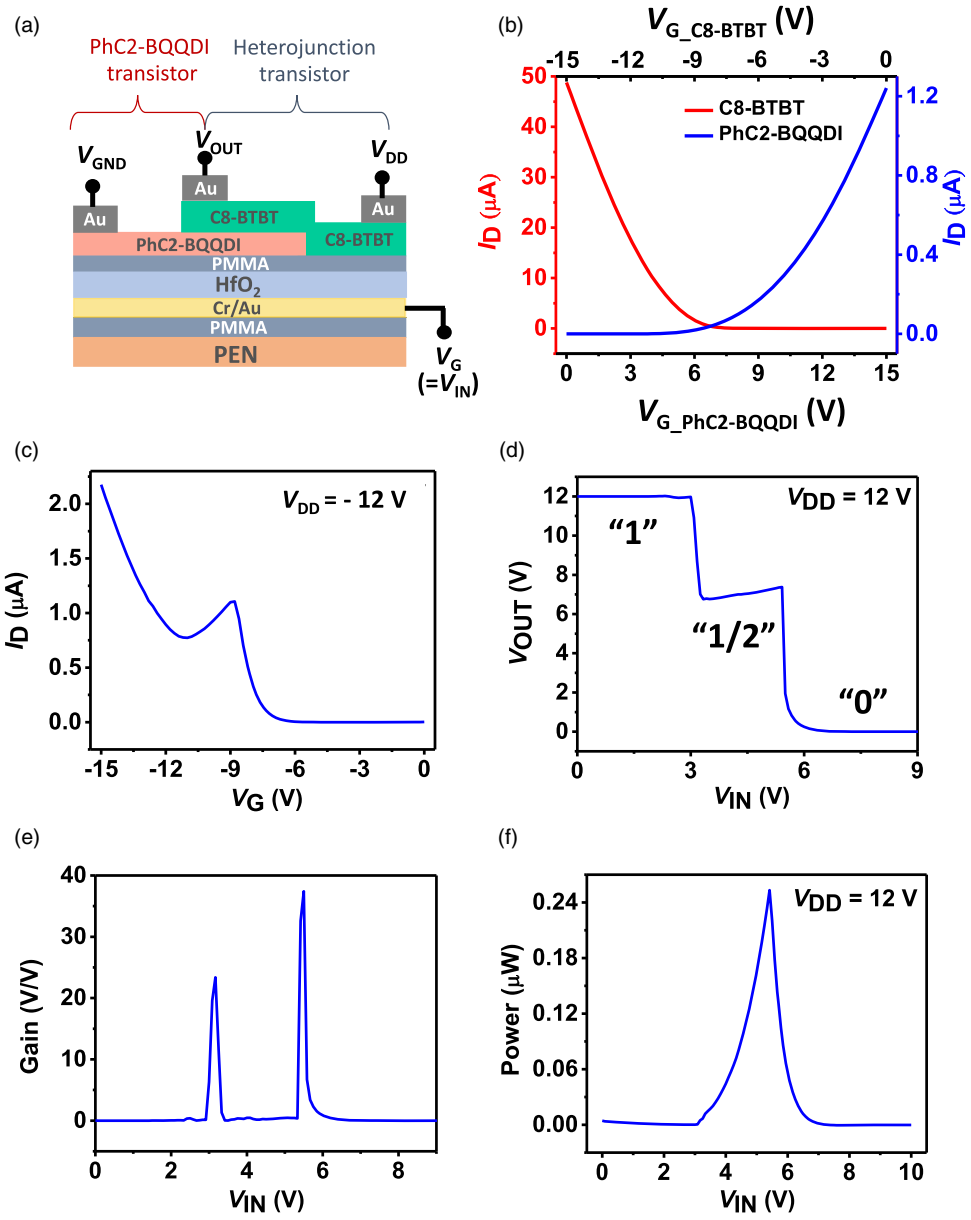

Fig.3. (Color online) (a) Schematic illustration of the ternary inverter with HfO_2 dielectric layer. (b) Transfer characteristics (at $V_D = |12|$ V) of the C8-BTBT (red line) and PhC2-BQQDI (blue line) transistors. (c) Transfer curve of the heterojunction transistor at $V_{DD} = -12$ V. (d) Voltage transfer characteristics of the ternary inverter at $V_{DD} = 12$ V. (e) DC voltage gain and (e) static power consumption of the ternary inverters as a function of input voltage.

Although a slight shift in the voltage transfer curve (VTC) toward a higher V_{IN} was observed at $R_c = 6.6$ mm, the voltage levels of the three logic states and logic ½ width remained close to constant, as shown in Fig. 2(c). This is because the bending induced a V_{th} shift only in the C8-BTBT channel, whereas no variation was induced in the PhC2-BQQDI channel, as shown in the supporting information (Fig. S3). The VTCs clearly demonstrated ternary logic states even under the more stringent condition of $R_c = 5$ mm. These results indicate that the devices can withstand applied mechanical strain, even at an R_c of 5 mm. This corresponds to a tensile strain (ε) of 1.25%, which was calculated from $\varepsilon = t/2R_c$, where t is the thickness of the PEN substrate (125 μm). The tolerance of the devices to repeated bending was then tested at $R_c = 5$ mm. The VTCs in Fig. 2(d) were virtually unchanged, even after 100 bending cycles. The variation in the V_{OUT} levels and widths of the logic states are plotted as a function of numbers of bending cycles in Figs. 2(e) and 2(f), respectively. The V_{OUT} levels and widths of logic 1 and logic ½ states are denoted as V_{OUT} (1), *Width* (1), V_{OUT} (½) and *Width* (½), respectively [see Fig. 1(e)]. V_{OUT} (1) showed no variation with the bending cycle and remained constant at 60 V, whereas the V_{OUT} (½) showed a marginal change of 2% after 100 cycles. For the logic state widths, both *Width* (1) and *Width* (½) remained almost constant at 17.5 ± 0.3 V and 3.6 ± 0.4 V, respectively. These results clearly exhibit another merit of our devices, that is, their high mechanical bendability, which is necessary for flexible electronic applications.

Here, it should be noted that one challenge remained: the device requires a high driving voltage ($V_{DD} = 60$ V) for inverter operation. This problem was resolved by taking advantage of the high-k HfO_2 ($k \approx 19$) dielectric layer.[29] It is well known that high-k dielectric layers induce a high charge-

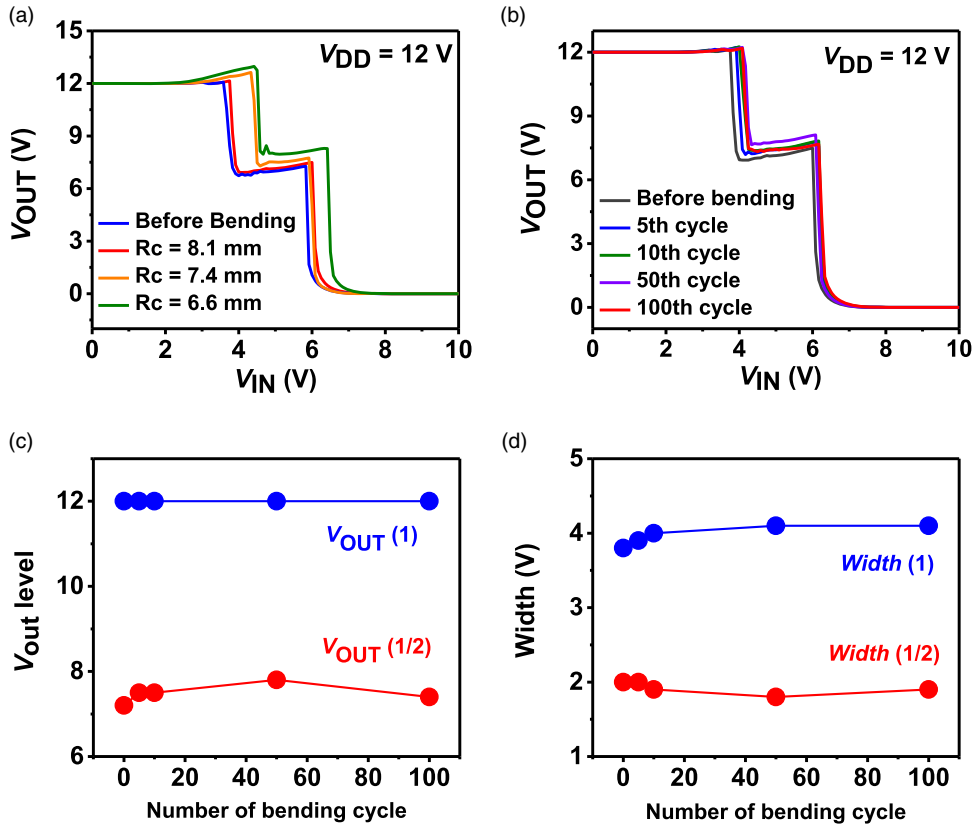

Fig. 4. (Color online) (a) Voltage transfer curves of the inverters as a function of bending radii (d) VTCs as a function of bending cycles at $R_c = 8.1$ mm. Variations in (e) output voltage levels and (f) logic state widths as a function of bending cycle. [Before Bending -> Before bending; Number of bending cycle -> Number of bending cycles.]

carrier density at the dielectric/semiconductor interface and thus can effectively reduce the operation voltage of the transistors.[30,31] A schematic illustration of the inverter configuration is shown in Fig. 3(a). Here, a 30 nm thick HfO_2 layer was deposited on top of the gate electrodes layer by atomic layer deposition using tetrakis(dimethylamino) hafnium (TDMAH) as the hafnium precursor and water as the oxygen source. A 10 nm thick PMMA layer was deposited on the HfO_2 coating as a surface treatment designed to passivate the interfacial carrier traps and to facilitate charge transport at the dielectric-semiconductor interface.[30,32]

Figure 3(b) shows the transfer curves of the PhC2-BQQDI (blue line) and C8-BTBT (red line) transistors with the HfO_2 dielectric layer. The threshold voltages (V_{th}) of both transistors were effectively reduced to 6 V and –8 V, respectively. In response to the reduction of V_{th}, the HT and ternary inverter attained low-voltage operation, as observed in Figs. 3(c) and 3(d), respectively. The HT showed a high peak current (I_{peak}) of 1 μA at $V_G = V_{Peak} = -9$ V. I_{on} of 2 μA was obtained at $V_G = 15$ V, yielding the on/off ratio of 10^6 ($I_{off} = 3$ pA at $V_G = -2.8$ V). Moreover, a wide NDT range from −9 to −11 V was realized under the drain bias voltage V_{DD} of −12 V. Due to these superior electrical properties of the constituent transistors, the inverters also exhibited high performance, including full-swing operation and well-balanced ternary states: logic 1 at $V_{OUT} = V_{DD} = 12$ V, logic ½ at $V_{OUT} \approx V_{DD}/2 = 7$ V and logic 0 at V_{OUT} = ground. Interestingly, the DC gain values were further improved to 23.4 V/V and 37.5 V/V at $V_{IN} = 3.2$ V and 5.5 V, respectively, as shown in Fig. 3(e). In addition to low-voltage operation, use of the HfO_2 layer afforded another advantage: lower static power consumption. The power consumption (P) of the inverter was calculated from $P = (V_{DD} \times I_{GND})$ and is plotted as a function of V_{IN} in Fig. 3(f). The peak power consumption of the HfO_2-based device was found to be only 240 nW, which is almost one order less than the maximum power consumption of the inverter with the PMMA dielectric layer (see Fig. S4 in the supporting information). These results clearly demonstrate the application potential of the HfO_2-based organic MVLs in low-power ICs.

Finally, we examined the impact of substrate bending on HfO_2-based inverters. Similar to PMMA-based devices, we carried out bending tests at different bending radii to determine the tolerance limit of the devices. As shown in Fig. 4(a), the inverter characteristics remained almost unchanged after an applied bending radius of 8.1 mm. However, the VTCs showed pronounced shifts towards higher V_{IN} along with a deformation in the V_{OUT} (1) on decreasing the R_c, indicating that the devices can withstand bending down to a radius of 8.1 mm. The mechanical robustness of the devices was then tested by applying 100 bending cycles at $R_c = 8.1$ mm, as shown in Fig. 4(b). The VTCs of the inverters displayed very stable behavior in the cyclic bending test. Figures 4(c) and 4(d) respectively show the bending cycle-induced variation of V_{OUT} levels and the widths of the logic states. V_{OUT} (1) was found to remain constant at 12 V, regardless of the numbers of bends, that is, full-swing operations were maintained. On the other hand, V_{OUT} (½) showed slight fluctuation with bending cycles with a

maximum of an 8% change at the 50th bending. *Width* (1) and *Width* (½) also showed negligible variation with bending cycles and remained constant at 4 ± 0.2 V and 1.9 ± 0.1 V, respectively, demonstrating the high reliability of the HfO_2 devices under moderate bending conditions.

In summary, we have developed organic ternary logic circuits on flexible PEN substrates. First, the inverters were fabricated using a PMMA dielectric layer to prioritize mechanical flexibility. The devices showed three distinct, well-balanced logic states with high voltage gain and full-swing operation. The most important advantage of the devices was their ability to tolerate a tensile strain of up to 1.25%. However, the devices required a supply voltage of 60 V for inverter operation. This drawback was tackled by taking advantage of the high-k HfO_2 dielectric layer to investigate the potential for low-voltage operation. The HfO_2-based inverter was operable at 12 V. The devices also proved very resistant to an applied tensile strain of up to 0.78%, and displayed stable operation after 100 bending cycles. Both devices exhibited their own merits and can, accordingly, be utilized in different potential applications. This work, therefore, paves a realistic path towards the development of flexible and low-power organic MVLs for next-generation conformable logic applications.

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