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Dual-Gate Anti-Ambipolar Transistor with Van der Waals ReS_2/WSe_2 Heterojunction for Reconfigurable Logic Operations

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A dual-gate anti-ambipolar transistor (AAT) with a two-dimensional ReS_2 and WSe_2 heterojunction is developed. The characteristic Λ-shaped transfer curves yielded by the bottom-gate voltage are effectively controlled by the top-gate voltage. This feature is applied to logic operations, with the bottom- and top-gate voltages acting as two input signals and the drain current (I_d) monitored as an output signal. Importantly, a single dual-gate AAT exhibits all the two-input logic operations (AND, OR, XOR, NAND, NOR, and XNOR) under optimized input voltages. Additionally, drain voltage (V_d)-induced switching between AND and OR logic operations is achieved. These features are advantageous for simplifying circuit design.

1. Introduction

Beginning with the emergence of graphene,[1–3] the device applications of various two-dimensional (2D) layered materials, including transition metal dichalcogenides (TMDCs), have attracted much attention, and many related studies have been reported.[4–8] In particular, TMDCs can be utilized as transistor channels owing to their various band structures, and thus are expected to be utilized in a variety of functional devices. The 2D materials are layered compounds with atomically flat surfaces, in which each layer is stacked with weak van der Waals interaction. Therefore, various combinations of materials are available for forming heterojunctions without the lattice mismatch limitation. This characteristic is very useful in developing anti-ambipolar transistors (AATs). AATs have a unique structure: n- and p-type semiconductors are overlapped at the center of the transistor channel[9] to make direct contact with no depletion layer. There are numerous studies of AATs, respectively utilizing organic semiconductors,[10–12] 2D TMDCs,[13–16] and combinations of these materials.[17,18] The uniqueness of AATs can be ascribed to the Λ-shaped transfer curves. The I_d increases from a certain voltage, and then decreases with increasing gate bias voltage, a behavior similar to that of negative differential resistance (NDR). Although NDR devices have been expected to be key elements of logic circuits since the invention of the Esaki diode,[19] no practical device has yet been developed, because cryogenic temperatures are necessary for device operation and the peek-to-valley ratio (PVR) is only about 30 at room temperature,[20] which is insufficient for practical applications. In contrast, AATs can achieve high PVRs of 10^3–10^5 even at room temperature.[17,21,22] Therefore, AATs are strong candidates for use in new NDR devices, and multi-valued logic circuits have, in fact, been developed by taking advantage of this feature.[11,23] The present study exploited the NDR property to enable two-input logic operations, through the construction of a dual-gate AAT with an ReS_2/WSe_2 heterojunction. An important feature of the study was that all the two-input logic operations (AND, OR, XOR, NAND, NOR, and XNOR) were demonstrated using a single dual-gate AAT owing to its reconfigurable characteristics. Conventionally, a large number of transistors are required for conventional CMOS-based logic circuit technology (e.g., 12 transistors for a complementary-type XOR gate). In contrast, the reconfigurable dual-gate AAT offers a novel device architecture for the simplification of logic circuits and improvement in integration density.

Reconfigurable field-effect transistors are electronic devices that can reversibly change their conduction modes between p-type and n-type.[24–27] Such operation is available by plural gate electrodes those are program (or polar) and control gates. The program gate is to change the conduction modes between n- and p-type, and the control gate is to switch the field effect transistor (FET) between on and off states. Importantly, the conduction mode conversion is induced by electrostatic doping, i.e., electrons or holes are injected into the transistor channel by external bias voltage and, therefore, the channel materials are intrinsic semiconductors. Various materials have been reported for transistor channels, such as carbon nanotubes (CNTs)[28] Si nanowires,[29,30] graphene,[31] and transition metal

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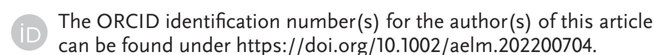
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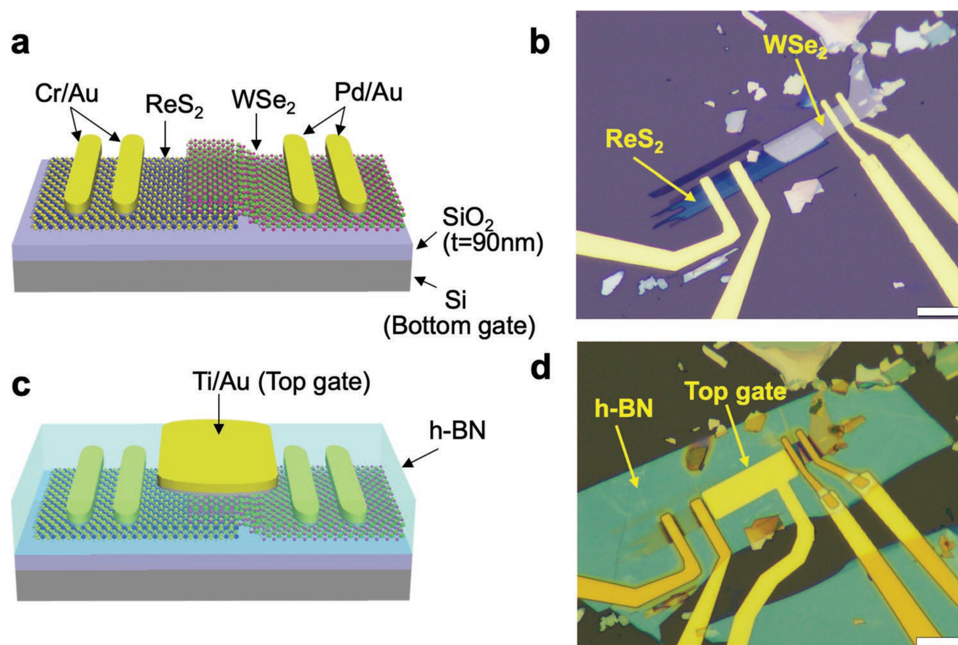

Figure 1. a) Schematic illustration and b) optical microscope image of a bottom-gate ReS_2/WSe_2 AAT. Scale bar: 10 µm. c) Schematic illustration and d) optical microscope image of the dual-gate ReS_2/WSe_2 AAT. The h-BN thin film was used as an insulating layer for the top gate. Scale bar: 10 µm.

dichalcogenides.[32] Although there have been many reports on logic operations using 2D materials,[33–36] in this study, we developed a new type of reconfigurable device based on the AAT. Here, the heterojunction with transition metal dichalcogenides plays crucial role to change the type of logic operation by optimizing the input bias voltages.

2. Results and Discussions

The heterojunction was fabricated by using ReS_2 and WSe_2 as the n-type and p-type semiconductors, respectively. Figures 1a,b respectively show a schematic illustration and an optical microscope image of a bottom-gate AAT. Cr/Au (5/100 nm) and Pd/Au (20/80 nm) electrodes were connected to the ReS_2 and WSe_2 channels, respectively, to investigate the electrical properties of the individual ReS_2 and WSe_2 transistors and those of the AAT. The channel length and width were 21.0 and 4.9 µm, respectively. The length of the overlapping area was 10.0 µm. The film thickness of the ReS_2 and WSe_2 was 4.8 nm (6 layers) and 10.0 nm (15 layers), respectively. **Figure 1**c shows a schematic illustration of a dual-gate AAT, with a hexagonal boron nitride (h-BN) film of 29.5 nm thickness covering the entire device and working as a top-gate dielectric layer. Then, a Ti/Au (5/100 nm) electrode was patterned as a top-gate electrode to cover the entire channel area. Figure 1d shows an optical microscope image of the prepared dual-gate AAT.

The transfer curves of the ReS_2 (blue) and WSe_2 (red) field-effect transistors (FETs) are shown in **Figure 2**a. Here, the ReS_2 FET shows n-type characteristics, while the WSe_2 FET shows ambipolar characteristics. The threshold voltage of the ReS_2 FET (–10.6 V) was lower than that of the WSe_2 FET of the p-type conduction (–6.8 V), which satisfied the condition for demonstrating anti-ambipolar characteristics. The field-effect mobilities were determined to be 8.4 and 6.5 $cm^2\ V^{-1}\ s^{-1}$ for the ReS_2 and WSe_2 FETs, respectively. These comparable mobilities are advantageous for balancing the electron and hole transports.

Figure 2b shows the carrier transport characteristics of the ReS_2/WSe_2 AAT driven by bottom-gate voltage (V_{bg}) at a fixed drain voltage (V_d) of –3 V. The transfer curves are shown in linear (black) and log (blue) scales. A typical Λ-shaped curve with a peak at –6.7 V was observed in the V_{bg} range from –4 to –12 V, and the sharp and symmetric curve indicated good balance between the electron and hole transports. It should be noted that I_d increased again above 4 V of V_{bg}. This was due to the ambipolar characteristics of the WSe_2 FET; both the ReS_2 and WSe_2 FETs were in the on state in this range. The gate-bias dependence of the energy-level alignments is shown in Figure 2c, to explain the origin of the Λ-shaped characteristics. In the range around V_{bg} = –12 V, no electrical current was observed because the n-channel was non-conductive. Similarly, no electrical current was observed in the range around V_{bg} = –2 V because the p-channel was non-conductive. Both the n- and p-channels were in the on state only in the middle range from –4 to –12 V. As a result, a sharp increase and decrease in I_d was induced, with monotonically increasing V_{bg}, to yield the Λ-shaped curve.

Next, we examined the effect of the top-gate bias voltage (V_{tg}) on the transfer curve. Figure 2d shows the variation in the transfer curve when the V_{tg} was applied from –4.9 V (red) to –2.7 V (dark blue). Figure 2e shows the V_{tg} dependence of the peak voltage (V_{peak}) and peak width (ΔV). Here, ΔV was defined as a peak width at $|I_d|$ = 0.2 nA. The V_{peak} exhibited clear dependence on the V_{tg}, shifting from –7.0 to –8.9 V. On the other hand, ΔV around 1.1 V was almost constant throughout the whole V_{tg} range. These results indicate that the threshold voltage of

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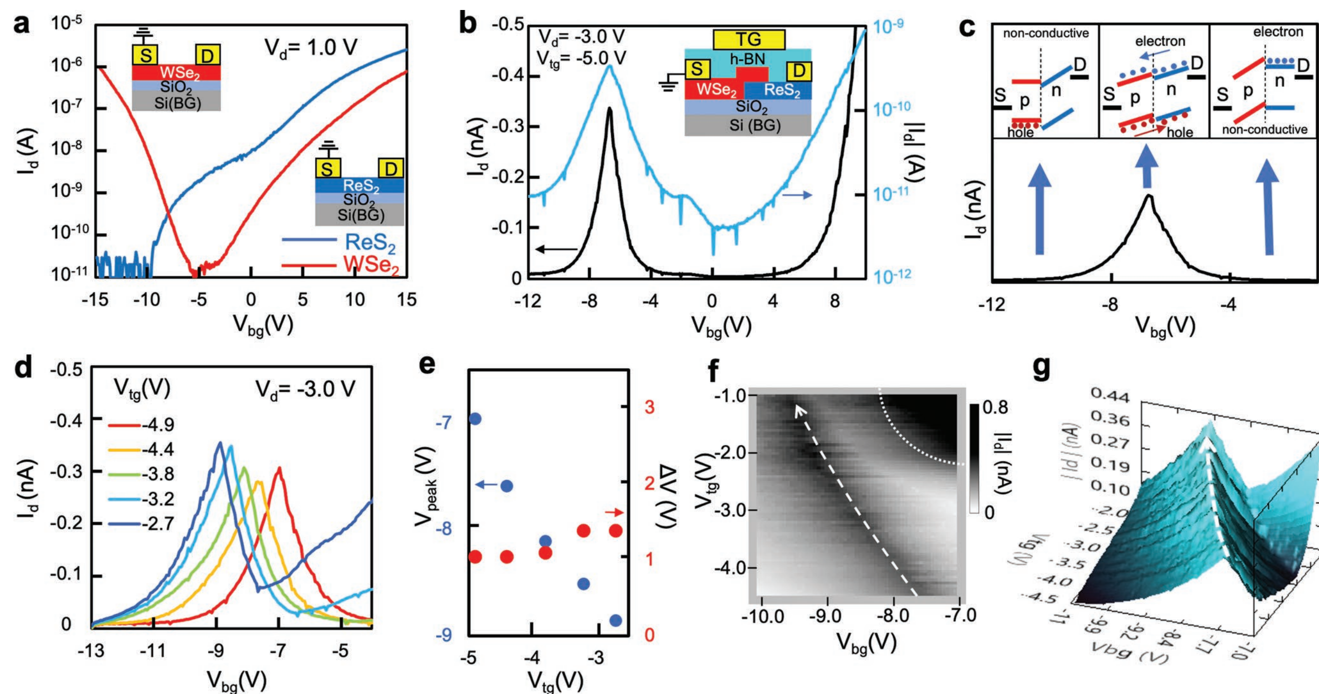

Figure 2. a) Transfer characteristics of the ReS_2-FET (blue) and WSe_2-FET (red). b) Λ-shaped transfer characteristics of the ReS_2/WSe_2 AAT. c) Energy-level alignments depending on gate bias voltage (V_{bg}), and the Λ-shaped transfer curve. d) V_{tg} dependence of the transfer characteristics. e) V_{tg} dependence of the V_{peak} and peak width (ΔV) at $|I_d|$ = 0.2 nA. f) 2D and g) 3D plots of I_d against V_{bg} and V_{tg}. The V_{peak} was shifted by V_{tg}, as indicated by the dashed lines.

both the ReS_2 and WSe_2 FETs shifted equally depending on the V_{tg}. Figures 2f,g respectively show two-dimensional and three-dimensional plots of I_d against V_{bg} and V_{tg}. The V_{peak} of the AAT shifted continuously, as indicated by the dashed lines. Additional intensive electrical current was observed around the upper right corner, as shown by the dotted arch in Figure 2f. This was also due to the ambipolar characteristics of the WSe_2 FET. These properties are significant for the realization of logic gate operations.

Based on these features of the dual-gate AAT, we developed two-input logic circuit operations. In **Figure 3**a,b, the bottom- and top-gate voltages act as input 1 (V_{IN1}) and input 2 (V_{IN2}), respectively, and I_d was monitored as the output. The absolute values of the output current are mapped against input voltage 1 (V_{IN1}) and 2 (V_{IN2}), with the current binarized at a threshold current of 0.2 nA. Here, current greater than 0.2 nA (gray area) is defined as the on-state "1" of the output, and current less than 0.2 nA (white area) is defined as the off-state "0" of the output. Figure 3a demonstrates an AND logic operation, in which V_{IN1} of −9.5 and −8.5 V were defined as "0" and "1" for input 1, and V_{IN2} of −4.7 and −3.5 V were defined as "0" and "1" for input 2, respectively. The output becomes on-state "1" only when both input 1 and input 2 are "1," indicating that the device operates as an AND circuit. Similarly, the OR operation was confirmed by changing the combination of input voltages as shown in Figure 3b. The logic operations driven by pulse voltage inputs are shown in Figure 3c,d. As shown in Figure 3c, the output current becomes larger than the threshold current of 0.2 nA only when both inputs are "1," which is the AND operation. Similarly, the OR operation was confirmed as shown in Figure 3d.

Here, it should be mentioned that spike noises were observed around 6 s in Figure 3c,d. We have conducted additional experiments to address noise margin issue by fabricating a new device. A h-BN layer was inserted at the SiO_2/ReS_2–WSe_2 interface (see Figure S1a–d, Supporting Information). AND and OR logic gates are shown in Figures S2a–d (Supporting Information) as typical device operations. Unlike Figure 3, no spike noise appeared in this device even when a pulse voltage was applied as shown in Figure S2c,d (Supporting Information) Thus, one can say that the spike noise appearing in Figure 3 is not an intrinsic problem because it can be completely eliminated by preparing high quality interface. The high quality interface is also effective in eliminating hysteresis in the transfer curves as shown in Figure S3 (Supporting Information).

Importantly, the dual-gate AAT can enable AND and OR circuits independently, based on the input bias voltages, as demonstrated here. In a similar manner, other two-input logic operations (NAND, NOR, XOR, and XNOR) were enabled by optimizing the combination of the V_{IN1} and V_{IN2} voltages as input 1 and input 2, respectively, as shown in **Figure 4**a–d. The various logic operations were demonstrated simply by applying appropriate input voltages for the respective logic operations in a single device. This can be achieved only by the AAT because it allows the electrical current to flow only in the limited gate voltage ranges. It should be noted that a single current peak in the Λ-shaped curve cannot enable an XNOR circuit. However, I_d increased again in the voltage range marked by the dotted arch in Figure 2f, producing another on-state "1" in the output, enabling XNOR operation, due to the ambipolar characteristics of the WSe_2 FET (Figure 4d). In sum, all the two-input logic

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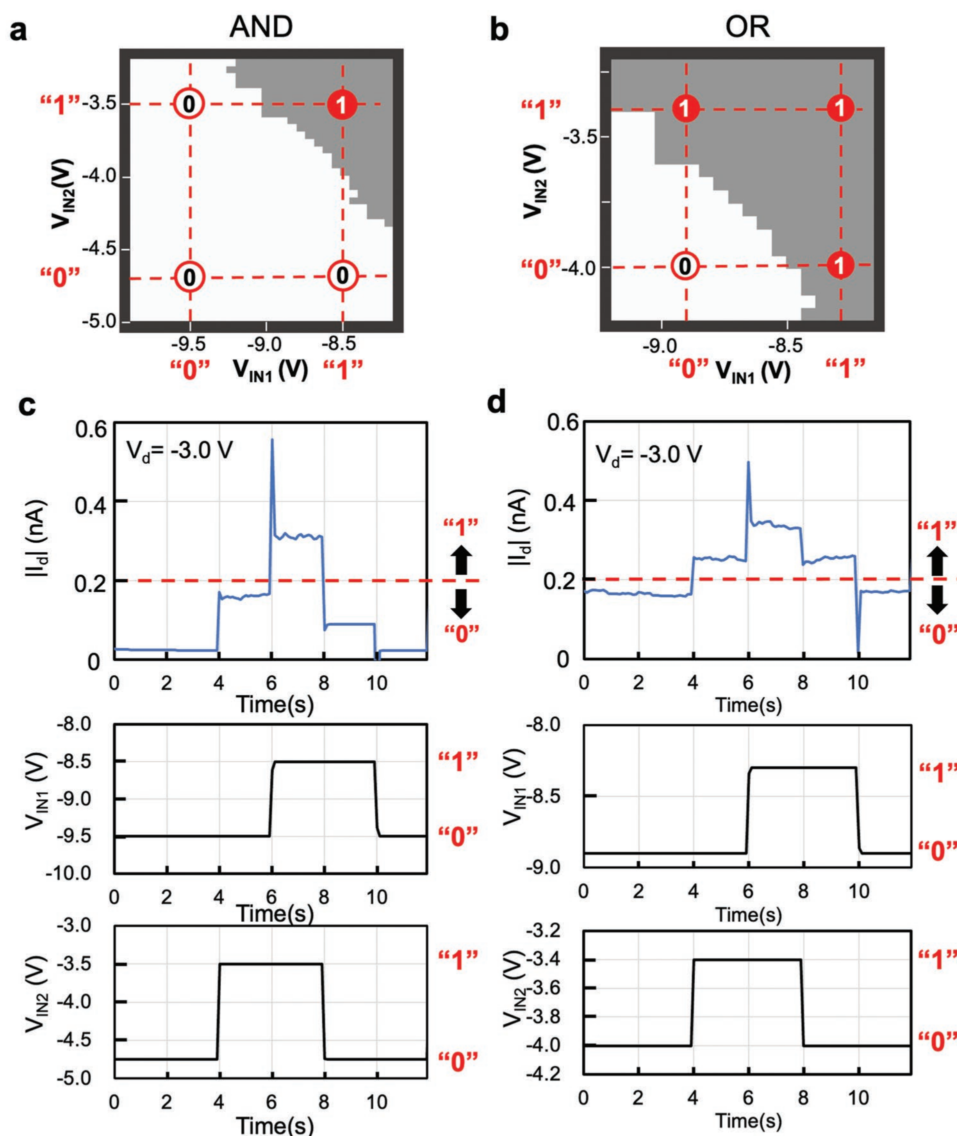

Figure 3. Logic operations of the dual-gate AAT. The logic circuits were operated with the bottom-gate voltage (V_{IN1}) as input 1, the top-gate voltage (V_{IN2}) as input 2, and the I_d as output. 2D binarized mappings of $|I_d|$ with a threshold current of 0.2 nA in an a) AND and b) OR circuit. Logic operations with pulse voltage input in a c) AND and d) OR circuit.

operations (AND, OR, XOR, NAND, NOR, and XNOR) were demonstrated. For the conventional logic operations, a number of transistors must be integrated (e.g., 4 transistors for NAND and NOR, and 12 transistors for XOR); however, the dual-gate AAT enabled all these operations in a single device architecture. Here, stable 2D mapping is necessary to guarantee the robustness of the logical input–output relationship. The stability of 2D mapping was investigated and the results was shown in Figure S4 (Supporting Information).

A further advantage of the AAT is its ability to operate at room temperature. Similar logic operations with a single device were reported by Majima et al.,[37] who developed single-electron transistors using gold particles, but a low-temperature environment was required for operation. By contrast, our device can work at room temperature, owing to the notable NDR of the AAT.

We also demonstrated another useful feature of the dual-gate AAT: switchable logic operations based on drain voltage. As shown in Figure S5 (Supporting Information), the current peak of AAT shifts depending on V_d. Therefore, by selecting the appropriate combination of V_d, it is possible to switch between different types of logic operations. **Figure 5**a–c shows experimental data for the AND operation: (a) wide-range 2D plots of $|I_d|$ against V_{IN1} and V_{IN2}; (b) binarized 2D plots of $|I_d|$ with a threshold current of 0.2 nA, the voltage range of which was extracted from the dotted square in Figure 5a; and (c) pulse input voltage operation. These were obtained at a V_d of −3.0 V. Figure 5d–f shows similar data for the OR operation; the only difference being the V_d of −3.5 V, with the other parameters (V_{IN1}, V_{IN2}, and threshold current) identical to those of the AND operation. Even the small variation in V_d, however, from −3.0 to −3.5 V, induced a drastic shift in the current peak, enabling

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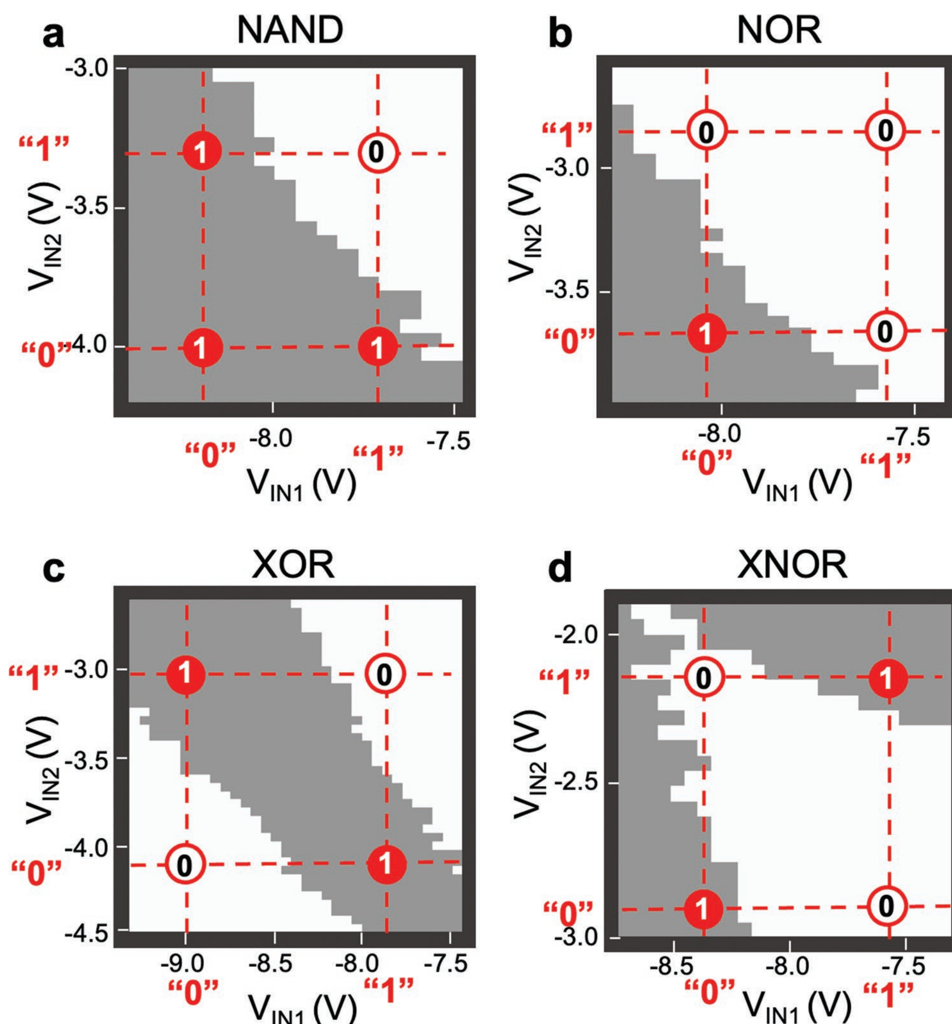

Figure 4. Various logic operations of the dual-gate AAT for a) NAND, b) NOR, c) XOR, and d) XNOR. These reconfigurable operations were enabled by appropriately optimizing the input voltages.

OR operation. These results indicate that variation in V_d can be effectively used to switch logic operations.

It should be referred that there are still challenges in our present work for further improvements. First, respective logic gates were operated at arbitrary input voltages, although the input voltage must be fixed at a certain value in actual logic circuits. To address this issue, the V_{peak} of AAT must be adjusted to fix the drive voltage. A possible way to realize this is chemical doping into the 2D materials,[38–40] and then the desired logic operations can be performed at a constant input voltage. Second, the input voltages were rather high, nearly 10 V. This value can be lowered by reducing the thickness of the dielectric layer and by using high-k dielectric materials.

3. Conclusion

We developed a multifunctional logic gate circuit based on a dual-gate AAT. The Λ-shaped transfer curve and ambipolar property of the WSe_2 FET were key factors. These factors depended on the bottom-gate voltage and were modulated by the top-gate voltage, enabling reconfigurable logic operations simply by optimizing the bias voltages. As a single device capable of performing all the two-input logic operations, the dual-gate AAT is expected to contribute to the simplification of circuit design and improvement in integration density.

4. Experimental Section

Device Fabrication: The ReS_2/WSe_2 heterojunction was fabricated using a bubble-free dry transfer technique.[41–43] The home-built transfer equipment consisted of an optical microscope (BX53M, Olympus Co.), manipulator, and heater. First, thin films of ReS_2 and WSe_2 were prepared from commercial bulk crystals (HQ Graphene) by the mechanical exfoliation method, using adhesive tape on highly doped Si substrate with a 90-nm thick SiO_2 layer. These films acted as a bottom gate and gate dielectric layer, respectively. TMDC flakes of a few nanometers in thickness were selected using optical microscopy, and the exact thickness, width, and length of the flakes were measured using an atomic force microscope (AFM). A combination of ReS_2 and WSe_2 flakes of comparable thickness, width, and length was selected, and the WSe_2 flake was stacked on the ReS_2 flake using the dry transfer method. A pair of Cr/Au (5/100 nm) electrodes, and another pair of Pd/Au

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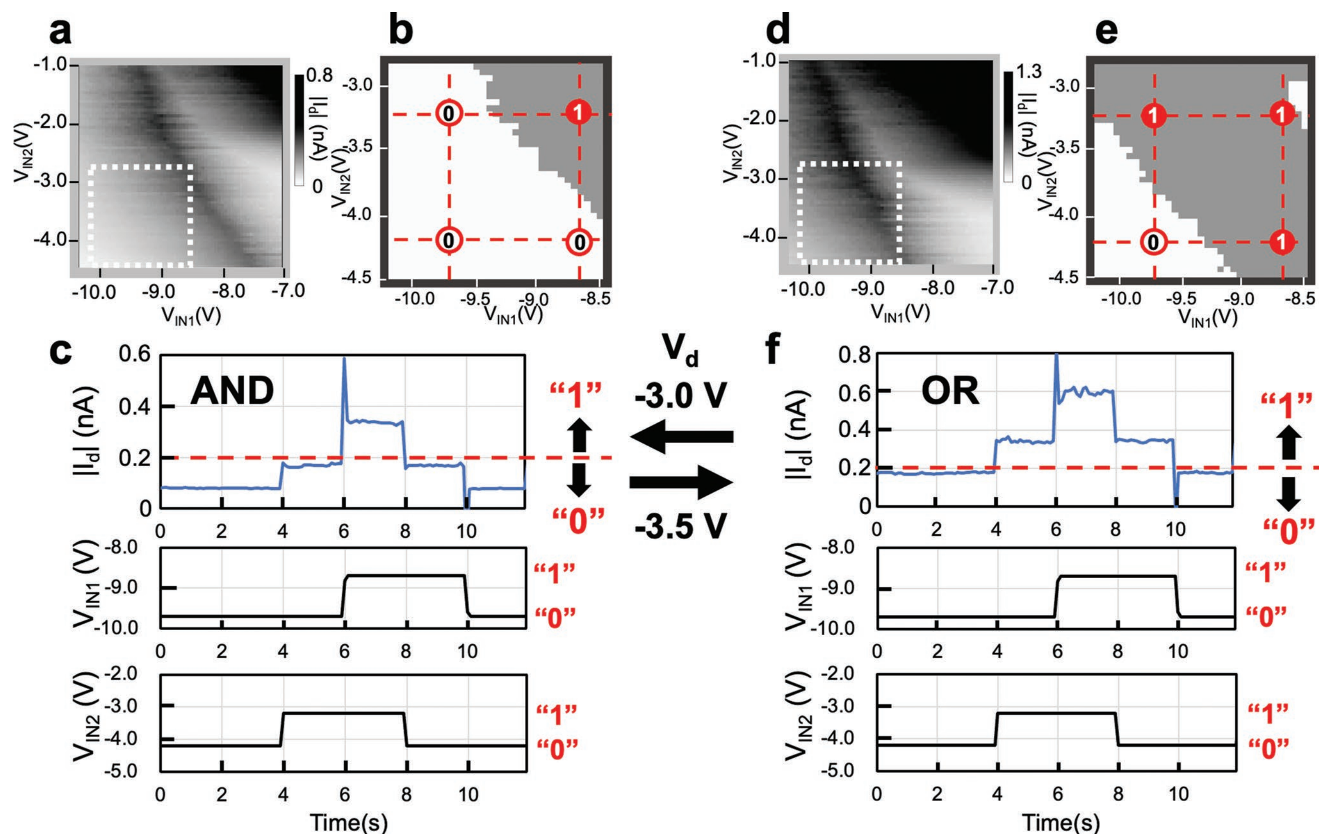

Figure 5. Switching between AND and OR operation by changing the drain voltage. a–c) AND operation at $V_d = -3.0$ V. d–f) OR operation at $V_d = -3.5$ V. Wide-range 2D plots of $|I_d|$ (a, d). Binarized 2D plots of $|I_d|$ extracted from the dotted squares in (a) and (d) (b, e). Logic operations with pulse voltage input (c, f).

(20/80 nm) electrodes, were put in contact with the ReS_2 and WSe_2 layers, respectively, using an electron beam evaporation and lithographic process. The Cr and Pd thin films were inserted to reduce the Schottky barrier in the contact area.[44,45] Subsequently, a h-BN film was stacked as the top-gate insulator, covering the entire device. Finally, a Ti/Au (5/100 nm) film covered the entire channel as the top gate. A Ti thin layer was inserted at the interface, for better mechanical bonding with the h-BN surface.

Device Characterization: The electrical characteristics of the device were measured in a vacuum (40 Pa) at room temperature using a probe station. The current–voltage and current–time characteristics were measured using source-measurement units (Agilent, B2912A, B2901A). An AFM (MFP-3D, Oxford Instruments) was used to measure the dimensions of the TMDC flakes, check the cleanliness, and remove the resist residues.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D materials, anti-ambipolar transistors, reconfigurable logic circuits, ReS_2, WSe_2

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