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Antiambipolar Transistor with Double Negative Differential Transconductances for Organic Quaternary Logic Circuits

*Debdatta Panigrahi, Ryoma Hayakawa, and Yutaka Wakayama**

Organic integrated circuits have emerged as potential candidates for next-generation computing technology because of their low-cost production, light weight, and mechanical flexibility. However, the incompatibility of organic devices with modern lithographic techniques leads to a major bottleneck, that is, low integration density. Herein, it is attempted to solve this issue by developing an organic quaternary inverter that exhibits four distinguishable logic states and thus, can significantly improve the level of device integration. The key component of the inverter is a double-peaked antiambipolar transistor (DAAT) with a double sequential negative differential transconductance characteristic. First, the DAAT is developed by employing two lateral p-n heterojunctions, namely C8-BTBT/PTCDI-C8 and C8-BTBT/PhC2-BQQDI, in which three distinct conducting paths are produced in a step-by-step manner in accordance with the increase in the gate voltage (V_G). Next, the quaternary inverter circuit is implemented by connecting the DAAT with an *n*-type transistor. The inverter exhibits four logic states with a complete drain voltage to ground voltage sweep. Finally, a strategy of optimizing the thickness of the PTCDI-C8 layer to improve the voltage transfer characteristics of the quaternary inverters is demonstrated. This study, thus, represents a step toward the development of high-performance organic integrated circuits.

1. Introduction

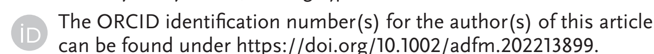
The upcoming generation of the Internet-of-things and artificial intelligence demands advanced computing technology that can efficiently process large quantities of data at high speed and with low power consumption.[1,2] Organic semiconductors offer enormous potential for use in such cutting-edge technologies because of their easily tuneable molecular properties, light weight and low production cost.[3,4] In addition, their intrinsic mechanical flexibility and solution processability make them suitable for state-of-the-art conformable neuromorphic computing applications.[5–8] However, organic devices suffer from a major bottleneck, that is, a lack of integration techniques. Conventional lithographic techniques cannot be applied to organic devices and therefore, organic integrated circuits still suffer from the difficulties of poor integration density and inadequate data processability.

The development of organic multi-valued logic circuits (OMVLs) has emerged as a promising solution to this problem. This is because MVLs can handle three or more logic states and consequently make it possible to realize higher information density with fewer interconnected devices.[9–15] Moreover, MVLs promote high-speed and low-power computation by reducing the number of interconnections, components, wiring density and overall system complexity. Recently, antiambipolar transistors (AATs) have been demonstrated for the realization of MVLs due to their negative differential transconductance (NDT) characteristics.[16–22] With AATs, ternary logic circuits can be implemented using only two transistors in contrast to the conventional CMOS technology where nine CMOS transistors are required to fabricate a ternary logic circuit.

Extensive efforts have already been made to develop high-performance organic ternary logic circuits in order to achieve the essential features required for their practical implementation, such as a complete drain voltage to ground voltage sweep, well-balanced logical states, high noise margin, low-voltage operation, mechanical flexibility and controllability of the device characteristics through external signals (such as light).[23–28] However, to expand the logic operation beyond ternary states and to further improve the integration density of the organic integrated circuits, it is necessary to establish advanced strategies and novel device architectures. Generating multiple NDT characteristics in the AATs is a promising way to solve this issue as AATs with multiple NDTs induce more than three logical states in the inverter circuits.

From these perspectives, we developed an organic quaternary logic circuit based on an AAT that exhibits two sequential NDT (bi-NDT) phenomena. Due to the presence of two "Λ"-shaped drain current (I_D) characteristics in the transfer curve, the transistor is termed a double-peaked AAT (DAAT). The DAAT was implemented using two vertically stacked *n*-type organic semiconductors, namely N,*N*′-dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C8) and PhC2H4-benzo[de]isoquinolino[1,8-gh]quinolone diimide (PhC2-BQQDI), and a *p*-type organic semiconductor, namely 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT). In the DAAT, the edges of both the PTCDI-C8 and PhC2-BQQDI

D. Panigrahi, R. Hayakawa, Y. Wakayama
International Center for Materials Nanoarchitectonics (WPI-MANA)
National Institute for Materials Science (NIMS)
1-1 Namiki, Tsukuba 305-0044, Japan
E-mail: wakayama.yutaka@nims.go.jp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layers form p-n heterojunctions with the edge of the C8-BTBT layer, thus constructing double lateral heterojunctions around the middle of the transistor channel. The bi-NDT in the DAAT was obtained from the two consecutive NDTs occurring at each lateral heterojunction. After realizing the bi-NDT characteristics, we configured a quaternary inverter by connecting the DAAT with an *n*-type transistor to achieve four distinguishable logic states, namely, "1", "2/3", "1/3", and "0".

This paper consists of four parts. The first part explains the carrier transport mechanism in the AAT. This part provides fundamental information about the bi-NDT of the DAAT, which is dealt with in the second part. In the third part, we demonstrate quaternary inverter operation by connecting the DAAT and *n*-type transistor in series. Finally, well-balanced quaternary logic states are achieved, where the film thicknesses are key factors in terms of controlling the widths of the four logic states.

2. Results and Discussion

First, we discuss the charge transport properties of a conventional AAT [29,30] with a single heterojunction consisting of C8-BTBT and PTCDI-C8. The chemical structures, surface morphologies of the C8-BTBT and PTCDI-C8 films and the electrical characteristics of both the transistors are shown in Figure S1a and b (Supporting Information). **Figure 1**a is a schematic illustration of the AAT, where a lateral heterojunction (highlighted by a dotted ellipse) of C8-BTBT and PTCDI-C8 layers is formed between the source and drain electrodes. The C8-BTBT layer is connected from source to drain to enhance the drain current (I_D) in the higher gate voltage (V_G) range.[23,26] Figure 1b shows the transfer characteristics of the AATs in the *p*-type operation. The transfer curve can be divided into four distinctive V_G ranges. In range (i) ($0 < V_G < -4.7$ V), the device

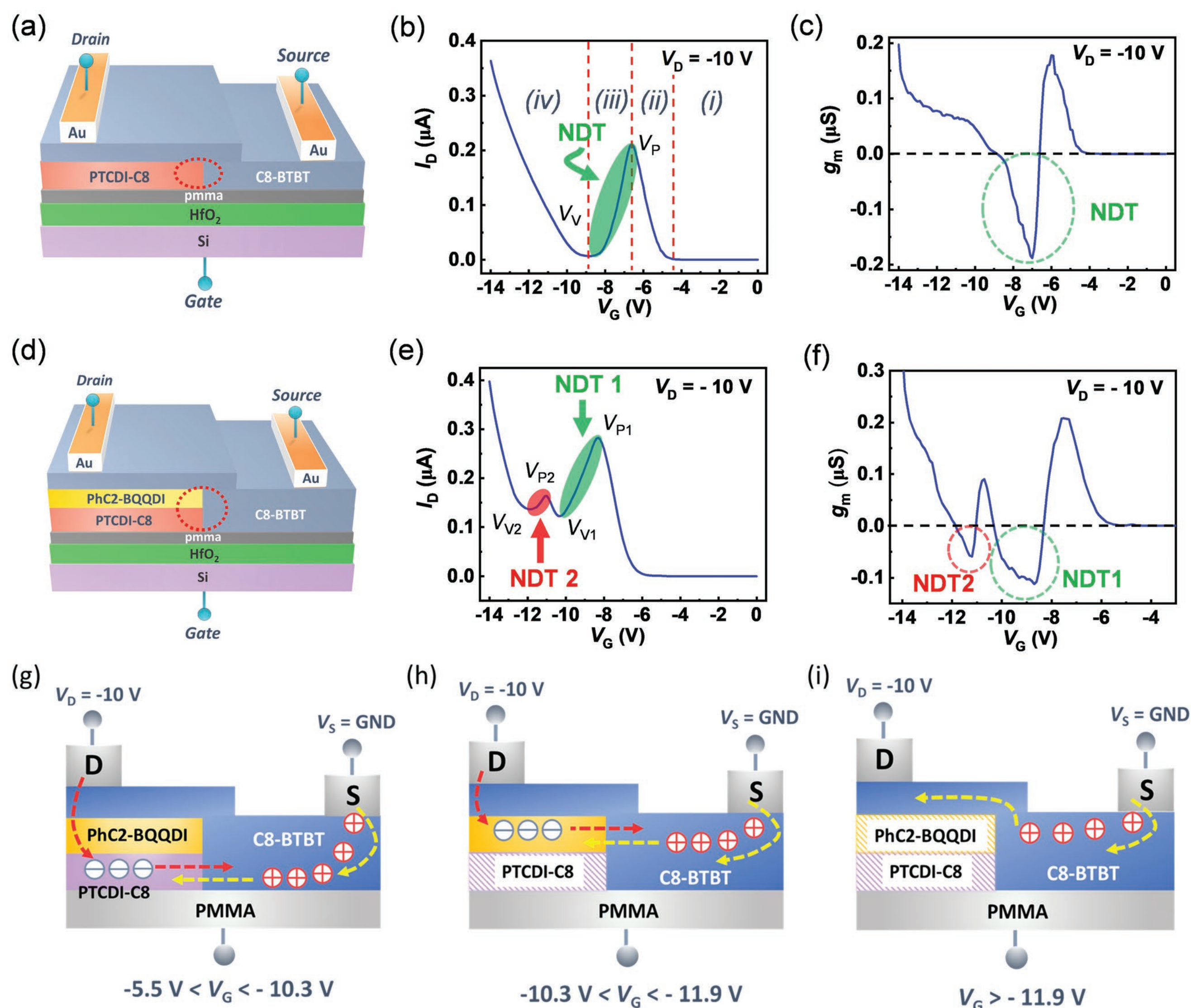

Figure 1. a) Schematic illustration of an AAT consisting of a C8-BTBT/PTCDI-C8 heterojunction. b) Transfer curve of the AAT at $V_D = -10$ V. c) Transconductance characteristics of the AAT as a function of V_G. d) Schematic illustration of a DAAT consisting of C8-BTBT/PTCDI-C8 and C8-BTBT/PhC2-BQQDI heterojunctions. e) Transfer curve of the DAAT at $V_D = -10$ V. f) Transconductance characteristics of the DAAT as a function of V_G. g–i) Charge conduction paths in the DAAT.

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remained in the off state because the applied V_G was insufficient to form the channel. In range (ii) (–4.7 V < V_G < –6.6 V), I_D started increasing with V_G due to the transport of holes and electrons across the heterojunction. In this range, the source to gate voltage (V_{SG}) induced a hole current in C8-BTBT ($I_{C8\text{-}BTBT}$), while the drain to gate voltage (V_{DG}) induced an electron current in the PTCDI-C8 layer ($I_{PTCDI\text{-}C8}$). Both the hole and electron currents contributed to the I_D. At V_G = V_P = –6.6 V, I_D reached a peak value of 210 nA (I_p) since the summation of $I_{C8\text{-}BTBT}$ and $I_{PTCDI\text{-}C8}$ reached its maximum value. In range (iii) (–6.6 V < V_G < –8.9 V), an NDT characteristic was observed; I_D started decreasing as V_G increased. This NDT characteristic is due to the depletion of the PTCDI-C8 channel. In this V_G range (NDT range), I_D was reduced from the peak current of 210 nA to a valley current (I_V) of 5 nA at V_G = V_V = –8.9 V. Finally, in range (iv) (–8.9 V < V_G < –14 V), I_D started increasing again due to the flow of holes through the continuous C8-BTBT layer and attained an on current (I_{on}) of 360 nA at V_G = –14 V. In this way, the transport properties of the AAT are controlled by two conductive pathways. One is the lateral heterojunction, which dominates over V_G ranges (ii) and (iii), yielding the NDT behavior. The other is the continuous C8-BTBT layer, which governs the I_D enhancement in range (iv) after the depletion of the PTCDI-C8 layer. Figure 1c shows the transconductance (g_m) characteristics of the AAT. The maximum NDT value (g_{max}) of 0.19 µS was obtained at V_G = –7 V.

These discussions about the AAT are helpful as regards understanding the carrier transport mechanism in the DAAT. The DAAT is composed of dual *n*-type layers of PhC2-BQQDI and PTCDI-C8, and a *p*-type layer of C8-BTBT. The chemical structure, surface morphology of the PhC2-BQQDI layer and electrical characteristics of the transistor are shown in Figure S1c (Supporting Information). Figure 1d is a schematic illustration of the DAAT, in which vertically stacked PhC2-BQQDI and PTCDI-C8 layers form two lateral heterojunctions with the C8-BTBT layer as indicated by a dotted ellipse. The C8-BTBT layer is connected from source to drain electrodes. Figure 1e shows the transfer characteristic of the DAAT in the *p*-type operation. In contrast to the single NDT in the AAT, the DAAT showed double consecutive NDT characteristics. The first was in the V_G range (NDT1 range) from –8.3 V (V_{P1}) to –10.3 V (V_{V1}) as highlighted in green. Here, I_D was reduced from 283 nA at the first peak voltage (V_{P1} = –8.3 V) to 110 nA at the first valley voltage of V_{V1} = –10.3 V. The second was in the V_G range (NDT2 range) from –11.0 V (V_{P2}) to –11.9 V (V_{V2}) as highlighted in red. Here, I_D was reduced from 153 nA at the second peak voltage (V_{P2} = –11.0 V) to 123 nA at the second valley voltage of V_{V2} = –11.9 V. Figure 1f shows the NDT profile of the DAAT as a function of V_G. Two NDT peaks of g_{m1} = 0.11 µS (NDT1) and g_{m2} = 0.06 µS (NDT2) were observed at V_G = –8.7 V and –11.3 V, respectively. I_D–V_G curves with different V_D and the NDT ranges depending on V_D are shown in Figure S2 (Supporting Information).

Figure 1g–i show the charge transport paths in the DAAT. Similar to the single heterojunction AAT, the DAAT was in the off state below V_G = –5.5 V showing no electrical current. Then, the increase in V_G resulted in channel formation in both the C8-BTBT and PTCDI-C8 layers just above the PMMA layer, initiating an electrical current. In a V_G range of –5.5 V < V_G < –10.3 V (= V_{V1}), the electron and hole were transported through the channel across the C8-BTBT and PTCDI-C8 heterojunction (Figure 1g), in which a peak drain current (I_{P1} = 283 nA) appeared at V_{P1} due to the optimum balance between $I_{C8\text{-}BTBT}$ and $I_{PTCDI\text{-}C8}$. In the NDT1 range (indicated in green), $I_{PTCDI\text{-}C8}$ was reduced due to the reduction of V_{DG}, making the PTCDI-C8 layer less conductive. In the range of –10.3 V (= V_{V1}) < V_G < –11.9 V (= V_{V2}), the PhC2-BQQDI/C8-BTBT heterojunction served as a conductive path for both electrons and holes (Figure 1h). Consequently, I_D increased again from I_{V1} to I_{P2}. I_{P2} represents the local maximum drain current of $I_{PhC2\text{-}BQQDI}$ and $I_{C8\text{-}BTBT}$. With a further increase in V_G above –11 V, the PhC2-BQQDI layer became less conductive while yielding NDT2 range (shown in red). Finally, in the high V_G range (–11.9 V < V_G < –14 V), I_D increased for the third time from I_{V2} (123 nA) to I_{ON} (400 nA) because the C8-BTBT layer worked as a continuous channel as shown in Figure 1i. Thus, three distinct conducting paths, namely two heterojunctions and the continuous C8-BTBT layer, were produced in a step-by-step manner in association with the monotonical increase in V_G. As a result, sequential NDT (bi-NDT) characteristics were yielded in the DAAT. The origin of the double I_D peaks in the DAAT was further confirmed by comparing the NDT characteristics, i.e., the bi-NDT in Figure 1e can be explained as an overlap of the transfer curves of the individual C8-BTBT/PTCDI-C8 and C8-BTBT/PhC2-BQQDI heterojunction-based AATs as shown in Figure S3 (Supporting Information). Here it is important to note that after the insertion of the PhC2-BQQDI layer in the DAAT, the Vp_1 in the DAAT was shifted to –8.3 V (Figure 1e) from Vp = –6.6 V in the AAT (Figure 1b). The reason behind the negative shift of the transfer curve in the DAAT can be attributed to the lower threshold voltage (V_{Th}) of the PhC2-BQQDI layer than that of PTCDI-C8. As shown in Figure S1b and c, PhC2-BQQDI transistor showed V_{Th} of 3 V whereas PTCDI-C8 transistor showed V_{Th} of 4.6 V. This result indicates that PhC2-BQQDI layer acts as an electron injection layer and therefore the electron current from the drain electrode to the PTCDI-C8 layer is enhanced. As a result, the transfer curve of the DAAT was shifted toward negative V_G compared to that of the AAT without PhC2-BQQDI layer.

The bi-NDT phenomena observed in the DAAT enabled us to configure the quaternary logic circuit. **Figure 2**a provides a schematic illustration and the circuit diagram of the quaternary inverter. The inverter circuit was constructed by connecting a DAAT in series with a PTCDI-C8/ PhC2-BQQDI double layered *n*-type transistor. The supply voltage (V_{DD} = 14 V) was applied to the drain electrode of the DAAT, and the input voltage (V_{IN}) was applied to the common gate electrode. The source electrode of the *n*-type transistor was grounded and the output voltage (V_{OUT}) was monitored at the middle-shared electrode. Figure 2b shows the voltage transfer characteristics (VTC) of the quaternary inverter. The inverter exhibited a complete V_{DD} (= 14 V) to ground (= 0 V) voltage swing with four clearly distinguishable logic states: logic "1" at V_{OUT} = 14 V, logic "2/3" at V_{OUT} = 11.4 V, logic "1/3" at V_{OUT} = 6.8 V and logic "0" at V_{OUT} = ground. The inverter was also able to yield sufficient voltage gain as shown in Figure 2c. Three peak values were observed in the gain profile of the inverter: 19.5 V/V at V_{IN} = 3.3 V (logic "1" to logic "2/3" transition point), 13 V/V at V_{IN} = 4.6 V (logic "2/3" to logic

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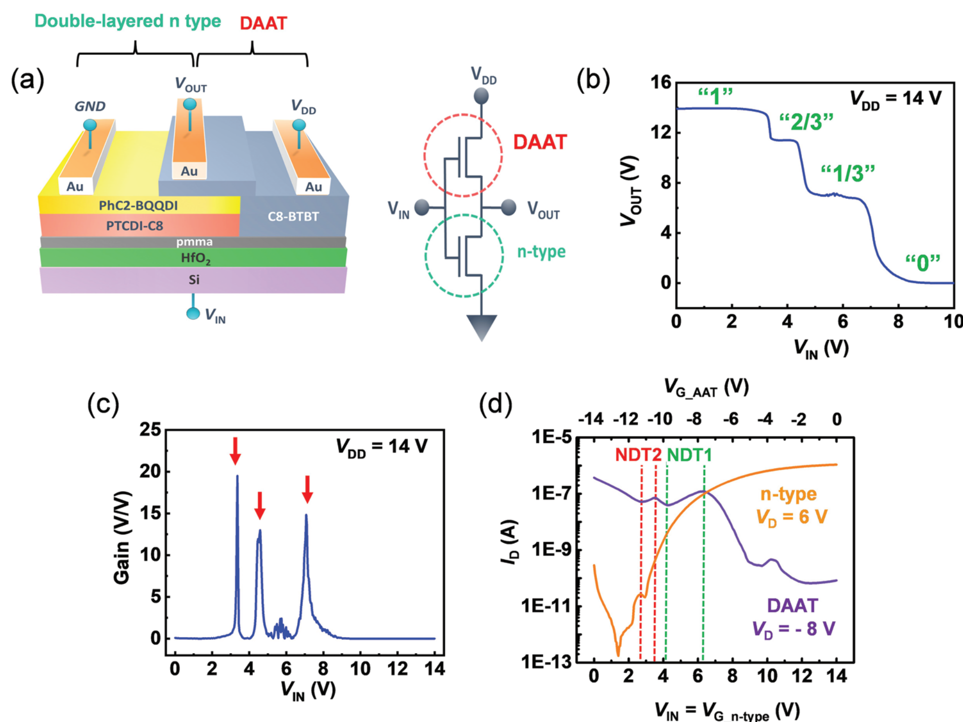

Figure 2. a) Schematic illustration and circuit diagram of a quaternary inverter consisting of a DAAT and a PTCDI-C8/PhC2-BQQDI double layer *n*-type transistor. b) Voltage transfer characteristics of the quaternary inverter at V_{DD} = 14 V. c) Voltage gain profile of the inverter as a function of applied input voltage. d) Transfer characteristics of the constituent DAAT and *n*-type transistor.

"1/3" transition point) and 14.5 V/V at V_{IN} = 7 V (logic "1/3" to logic "0" transition point) as indicated by the red arrows. The inverter operation can be explained from the transfer characteristics of the constituent DAAT and *n*-type transistors as shown in Figure 2d. In a low V_{IN} range ($0 < V_{IN} < 2.8$ V), where I_{D_DAAT} (I_D of DAAT) >> I_{D_ntype} (I_D of *n*-type transistor), V_{OUT} was equal to V_{DD} (logic "1") since a conductive path was established between V_{DD} and the output terminal. In the intermediate ranges, where $I_{D_DAAT} > I_{D_ntype}$ (in the NDT2 range of the DAAT) and $I_{D_DAAT} \sim I_{D_ntype}$ (in the NDT1 range of the DAAT), V_{DD} was divided into the two constituent transistors, which consequently yielded two middle logic states: logic "2/3" and logic "1/3". Finally, in the high V_{IN} range ($V_{IN} > 6.3$ V), where I_{D_ntype} >> I_{D_DAAT}, a conductive path was established between the output terminal and ground, which led to V_{OUT} = ground (logic "0"). Thus, the bi-NDT characteristic of the DAAT realized four discernible logic states that enabled the quaternary inverter operation.

Here, one challenge remains as regards the quaternary logic circuit, namely, the unbalanced width of the four logic states. In particular the width of the logic "2/3" state was only 0.9 V, which was rather narrow compared with the others: 2.8 V of logic "1" and 1.9 V of logic "1/3" states. This was due to the narrow NDT2 range observed in the transfer characteristics of the DAATs. Therefore, it was imperative to enlarge the NDT2 range to broaden the width of the logic "2/3" state and to achieve well-balanced quarternary logic states. A strategy for extending the NDT2 range is to suppress the hole current (I_{ON}) of the C8-BTBT layer in the high V_G range (-11.2 V < V_G < -14 V) in the DAATs (Figure 2d). In this V_G range, the $I_{C8\text{-}BTBT}$ flows in a vertical direction over the edge of the p-n junctions as illustrated in Figure 1i. Accordingly, any increment in the total thickness of the *n*-type semiconductor layers is expected to restrict the vertical transport in the C8-BTBT layer at the edge of the p-n junctions to extend the NDT2 range. For this purpose, we optimized the PTCDI-C8 layer ($T_{PTCDI\text{-}C8}$) in the 8 – 25 nm range. Then, we fixed $T_{PhC2\text{-}BQQDI}$ at 7 nm.

Figure 3a–c show the transfer characteristics of the DAATs with three different $T_{PTCDI\text{-}C8}$ values: 8, 14, and 20 nm. When $T_{PTCDI\text{-}C8}$ was increased from 8 to 14 nm, the NDT2 range was slightly extended from 0.9 to 1.2 V. This is a result of the reduction in I_{ON} from 407 nA ($T_{PTCDI\text{-}C8}$ = 8 nm) to 205 nA ($T_{PTCDI\text{-}C8}$ = 14 nm). With a further increase in $T_{PTCDI\text{-}C8}$ to 20 nm, I_{ON} decreased markedly to 9 nA. As a result, the NDT2 range was extended substantially from 1.2 to 2.6 V. Such significant broadening of the NDT2 range is attributable to the increased PTCDI-C8 thickness. Along with the NDT2 range, the NDT1 range was also found to increase gradually from 1.9 V at $T_{PTCDI\text{-}C8}$ = 8 nm to 2.7 V at $T_{PTCDI\text{-}C8}$ = 20 nm. The reason behind this improvement can be explained by the reduction in the threshold voltages ($V_{n,th}$) of the *n*-type transistor channels. To confirm the impact of $T_{PTCDI\text{-}C8}$ on the reduction in $V_{n,th}$, we measured the transfer characteristics of a PTCDI-C8/PhC2-BQQDI dual layer *n*-type transistor by varying the $T_{PTCDI\text{-}C8}$ value (Figure 3d). We observed that the $V_{n,th}$ gradually decreased from 5.1 to 4.6 V when $T_{PTCDI\text{-}C8}$ was increased from 8 to 20 nm, resulting an extension of the NDT1 range from 1.9 to 2.7 V. However, a further increase in $T_{PTCDI\text{-}C8}$ from 20 to 25 nm severely suppressed I_{ON} from 9 nA to 90 pA (Figure S4, Supporting Information). Thus, it was determined that a $T_{PTCDI\text{-}C8}$ of 20 nm is the optimized thickness for achieving the boarder width of both the logic "2/3" and logic "1/3"

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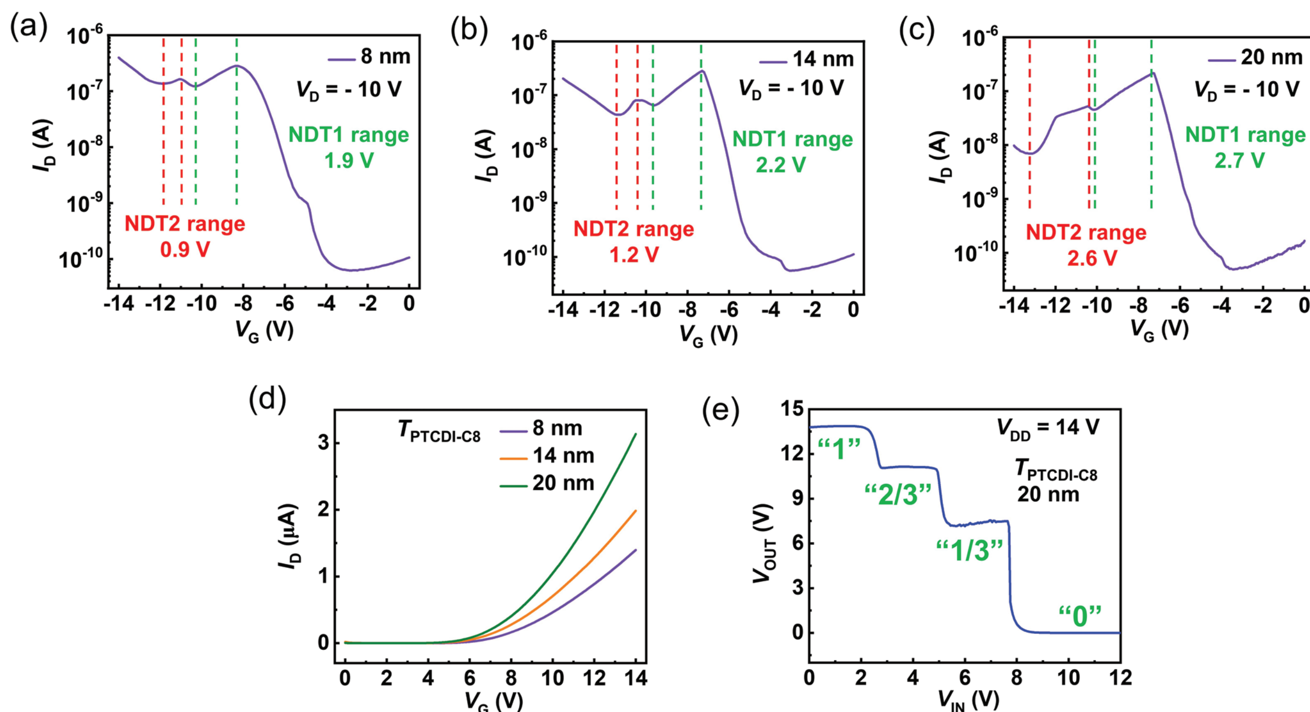

Figure 3. a–c) PTCDI-C8 layer thickness ($T_{PTCDI-C8}$) dependent transfer characteristics of the DAAT at $V_D = -10$ V. d) $T_{PTCDI-C8}$ dependent transfer characteristics of the PTCDI-C8/PhC2-BQQDI dual layer *n*-type transistor. e) Voltage transfer characteristics of the optimized quaternary inverter at $V_{DD} = 14$ V.

states. Here, it is important to note that along with $T_{PTCDI-C8}$ = 20 nm, the optimized $T_{PhC2-BQQDI}$ was also determined as 7 nm since any further increase in $T_{PhC2-BQQDI}$ severely degraded the NDT2 range (Figure S5, Supporting Information).

Next, we fabricated a quaternary inverter with the optimized $T_{PTCDI-C8}$ of 20 nm. Figure 3e shows the VTC of the optimized quaternary inverter. The corresponding transfer characteristics of the constituent DAAT and *n*-type transistors are shown in Figure S6 (Supporting Information). Post-optimization improvements in the NDT ranges were clearly reflected in the widths of the logic "2/3" and logic "1/3" states of the inverters. The width of the logic "2/3" state, which was originally only 0.9 V, was extended to 2.1 V. Meanwhile, the width of the logic "1/3" state was also enhanced from 1.9 to 2.3 V. Most importantly, the logic "1", "2/3" and "1/3" states showed almost the same width (2.2 ± 0.1 V) in the VTC inducing equiprobable accessibility to all the logic states. Thus, the proposed quaternary logic circuits achieved the following essential figures of merit: i) the realization of four clearly distinguishable logic states, ii) a complete V_{DD} to ground voltage swing, and iii) the equiprobable manifestation of the quaternary logic states. The operational stabilities of the DAAT and quaternary inverter are shown in Figure S7 (Supporting Information).

In work similar to ours, DAATs and quaternary inverters have been reported recently. Most of them are based on a 2D material platform, especially transition metal dichalcogenides (TMDCs), whereas organic semiconductors have remained unexplored.[31–36] 2D materials and organic semiconductors have some common merits, such as mechanical flexibility and dangling-bond-free surface properties. However, TMDCs suffer from a major disadvantage. The mechanical exfoliation technique used for the TMDC films hinders the reproducibility, size controllability, and scalability of the devices. The thermal evaporation technique used to produce organic semiconductor films provides an advantage in this respect. The device dimensions such as channel length and channel width, and the patterning of the channel layers can be controlled by using properly designed shadow masks. Furthermore, an input voltage as high as 100 V is required to generate four logic states in the 2D material-based quaternary inverter.[36] In contrast, the inverter proposed in this work achieved four logic states within a driving voltage of 14 V showcasing their compatibility in energy-efficient logic applications.

3. Conclusion

In conclusion, we have developed an organic DAAT, which exhibited two distinct NDT characteristics. The bi-NDT characteristics were achieved via the incorporation of two lateral organic heterojunctions, namely C8-BTBT/PTCDI-C8 and C8-BTBT/PhC2-BQQDI. Each heterojunction was capable of generating an NDT characteristic, which instigated the bi-NDT behavior in the DAATs. This unique bi-NDT feature enabled us to produce a quaternary inverter that can handle four logic states and thus, can significantly improve the data processing capability of the organic integrated circuits. For further improvement of the quaternary inverter performance, we verified the effectiveness of the thickness optimization; the optimized $T_{PTCDI-C8}$ and $T_{PhC2-BQQDI}$ realized well-balanced quaternary logic states. Consequently, the organic quaternary inverter designed in this work demonstrated its potential for next-generation data-intensive computing applications.

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4. Experimental Section

All the devices, including the transistors and quaternary inverters, were fabricated on highly doped *p*-type Si substrates, which worked as bottom gate electrodes. First, the substrates were cleaned by sequential ultrasonication with acetone, isopropanol and DI water. Then, using the atomic layer deposition (ALD) technique, a 30 nm-thick HfO_2 layer on the Si substrates was deposited where tetrakis(dimethylamino)hafnium (TDMAH) was used and water as hafnium and oxygen sources, respectively. On top of the HfO_2 surface, a thin layer (≈10 nm) of poly (methyl methacrylate) (PMMA) was spin-coated to passivate the surface defects and to facilitate the carrier transport through the organic channels.[24,37] Thereafter, two *n*-type organic semiconductors, PTCDI-C8 (≈8 nm) and PhC2-BQQDI (≈7 nm) were thermally evaporated consecutively at a background pressure of 10^{-7} Pa using a shadow mask. Next, a *p*-type C8-BTBT layer (≈25 nm) was thermally evaporated using another shadow mask to form a double lateral heterojunction in the DAATs. Finally, gold (Au) source and drain electrodes were deposited on the organic semiconductors with a thermal evaporation technique to complete the DAAT structure. The channel length and width of the DAATs were 100 and 350 µm, respectively. The quaternary inverters were implemented by connecting a DAAT in series with a PTCDI-C8/ PhC2-BQQDI dual layer n-channel transistor. All electrical measurements were performed in a vacuum (≈10^{-1} Pa) using an Agilent B1500A semiconductor parameter analyzer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

antiambipolar transistors, double negative differential transconductance, multi-valued logic circuits, organic semiconductors, quaternary inverters

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