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REGULAR PAPER

Fabrication of vertical-taper structures for silicon photonic devices by using local-thickness-thinning process

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This paper describes a simple fabrication process of vertical-taper structures which can locally tune the thickness of silicon photonic devices. For low-loss spot-size conversion, taper angles less than 10° are required. To fabricate the gradual-slope shape of the vertical tapers, we have developed a step-and-exposure lithography process, which is realized by repeated light exposure to photoresist and movement of the wafer stage by using commercial steppers. The process is conducted at a lower temperature (~120 °C) than the conventional process and is compatible with the complementary metal-oxide-semiconductor process. Also, we have made a model of the lithography to predict the angle of the taper. Theoretical angles are consistent with the experimental results. We demonstrate the conversion of a 400 nm thick silicon waveguide to 220 nm, whose length was 2.4 μm and insertion loss was measured to be less than 0.3 dB. The process enables us to choose the optimal thickness for each silicon-photonic device. © 2022 The Japan Society of Applied Physics

1. Introduction

Photonic integrated circuits (PIC) are expected to be used for many applications, e.g. data communication devices,[1–4] biosensors[5,6] and quantum computing.[7,8] To realize the PICs, silicon photonics is a promising technology[9–14] for its cost-effectiveness and integrability since it is fabricated by complementary metal-oxide-semiconductor technology. Recent foundry-based multi-project wafers for silicon photonic chips are typically fabricated by 220 nm thick silicon on insulator (SOI) platform,[14–17] and the platform has varieties of process design kits such as high-speed modulators, photodetectors and passive devices. However, the optimal thickness of silicon depends on its application.[18] For example, heterogeneous integration with III–V active devices,[19–21] which is important for indirect-bandgap material like silicon to integrate lasers or photodetectors, is usually realized by above 400 nm thick SOI platform to leverage evanescent coupling efficiently. In addition, around 110 nm thick and 260 nm thick SOI platforms are optimal for passive devices of quasi-TE polarization and TM polarization[18,22] since the platforms are tolerant against fabrication dimensional variations.[18] The thickness of silicon is also important for polarization control[23–25] or polarization-independent devices[26,27] because the effective indices of each mode depend on the thickness and width.

For these reasons, vertical tapers, which can convert the thickness of silicon waveguides, are a powerful tool to tune the thickness of silicon for each application and integrate them monolithically. To make the vertical taper, the fabrication of a gradual-slope shape is a challenge. Existing techniques need special processes and/or costly masks. For example, local oxidation of silicon-based process[28] requires silicon nitride hard masks and high temperature (1200 °C) annealing for a long time (>5 h), while shadow masked dry etching[29] requires special setups of etching equipment hence the process is not wafer-scale. The gray-scale photomask process needs costly photomask and experimental tuning of the geometry of the photomask.[30]

In this study, we present a simple fabrication process of vertical-taper structure that is realized by a combination of our step-and-exposure lithography[31,32] and dry etching. The process can realize the precise control of the thickness and the angle of silicon waveguides without annealing at high temperatures or special processes. In addition, we have made a model of the lithography, which can predict the angle of the tapers. Finally, we fabricated a taper that converts the 400 nm SOI waveguide to 220 nm with low-loss. The technique gives the seamless platform of silicon-photonic PIC, which can benefit from every advantage of each silicon thickness.

2. Design of waveguides and vertical tapers

The effective indices of silicon-channel waveguides were calculated using finite difference eigenmode analysis to figure out the variation in each silicon thickness. Figures 1(a) and 1(b) show the cross-section of silicon waveguides and effective indices of each mode of the waveguide, where TE_0 and TM_0 modes were calculated at a wavelength of 1310 nm and refractive indices of Si and SiO_2 are respectively 3.51 and 1.44. Effective indices increase as the thickness or width of silicon waveguides increases. As can be seen in Fig. 1(b), the effective indices change widely with thickness, which indicates that effective indices can be controlled by vertical tapers. For example, as the thickness varies from 220 to 1000 nm at the width of 400 nm, the effective index of TM_0 mode changes from 2.08 to 3.22 while that of TE_0 mode changes from 2.56 to 3.09. Thus, the tapers can also be applied to polarization diversity circuits or polarization-independent devices. The red line in Fig. 1(b) is an effective index of III–V lasers. As the width of the laser is wide (>2 μm),[9] the effective index of the laser is about 3.2. Therefore, a thickness of 400 nm or more is suitable for efficient evanescent coupling since the effective indices can be tuned to the laser, while 220 nm thick SOI cannot be tuned since the effective index cannot reach 3.2.

To design low-loss vertical tapers, we utilized the beam propagation method (BPM) for the quasi-TE mode at the wavelength of 1310 nm. Figure 2(a) represents the calculated transmission loss of vertical taper. The inset shows the simulation model of silicon vertical taper, whose width is 400 nm and cladding is silicon dioxide. The taper converts the thickness of the Si waveguide from 400 to 220 nm aiming

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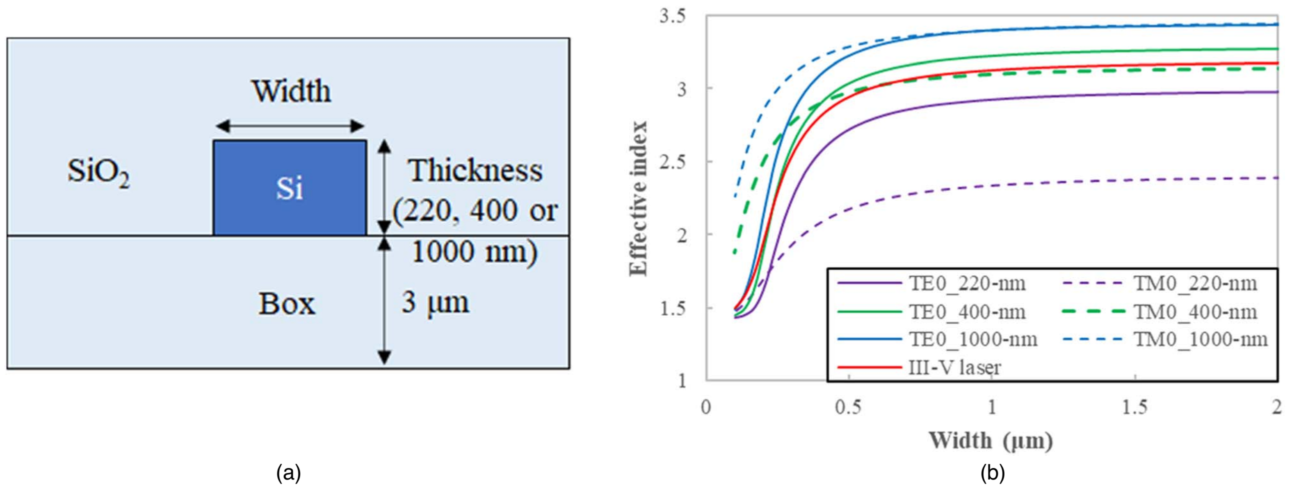

Fig. 1. (Colour online) (a) Cross-section of the silicon-channel waveguide. (b) Effective indices of silicon-channel waveguides for TE_0 (solid lines) and TM_0 (dashed lines) modes with 3 thicknesses (220 nm (purple), 400 nm (green) and 1000 nm (blue)). Redline represents the effective index of the III–V laser. The wavelength used in the simulation is 1310 nm, where the refractive indices of silicon, SiO_2 are 3.51 and 1.44, respectively. Refractive index of the III–V lasers is approximately set to the index of InP (3.2), whose thickness is 2 μm.

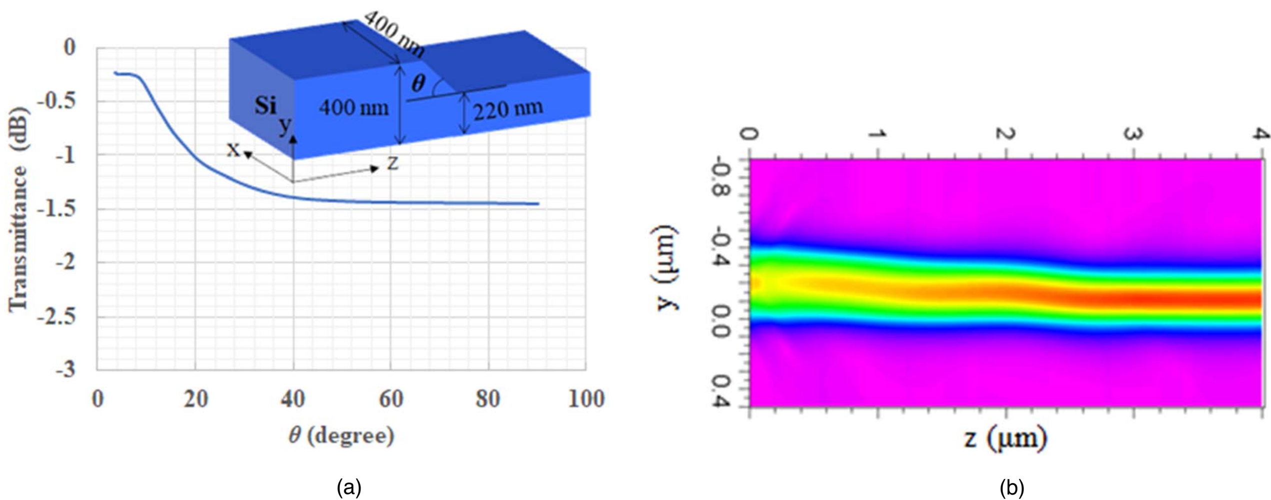

Fig. 2. (Colour online) (a) Transmission loss of the vertical taper from 400 to 220 nm calculated by BPM. The inset shows the simulation model and the background used in simulation is SiO_2, where the refractive indices of silicon, SiO_2 are 3.51 and 1.44, respectively. (b) Beam propagation of the taper at $\theta = 10°$.

to heterogeneously integrate III–V devices with the 220 nm platform. As can be seen in Fig. 2(a), transmission losses are low when θ is low, and the losses become higher as θ increases because of light leakage from the taper. To realize transmission loss less than 0.5 dB, θ should be less than 10°. Figure 2(b) shows the beam propagation along the taper (z-axis) at $\theta = 10°$. As the taper can convert the mode adiabatically, additional higher-order modes did not excite in the taper whose θ equals to 10° or smaller.

3. Principal and modeling of step-and-exposure lithography

To realize the gradual-slope shape of vertical tapers, we have developed step-and-exposure lithography by using a commercial stepper. Figure 3(a) shows the fabrication process flow of the vertical tapers. The process enables the formation of the vertical-taper structure in photoresist film and the pattern was transferred by the subsequent dry etching. In the exposure process drawn in Fig. 3(a-1), the photoresist is (i) exposed at weak (several mJ cm^{-2}) power, (ii) the wafer stage is moved by several μm and (iii) repeat the process (i) and (ii) until the amount of exposure become sufficient. After developing the photoresist (a-2), the stepwise shape is smoothed by baking the photoresist as shown in Fig. 3(a-3). The main feature of this process is the angle of the photoresist (θ_{PR}) and the slope (θ) can be controlled by the stepper.

To predict the angle of the slope, we have modeled the step-and-exposure process assuming the photoresist is linearly thinned to the amount of exposure. Figure 3(b) shows the amount of exposure and the thickness of the photoresist after developing. As the amount of exposure increase with the step, the photoresist starts to resolve from threshold-exposure power (P_{th}). The thickness of the photoresist is thinned as the exposure increases and completely develops from resolution-exposure power (P_{res}). Given photoresist thickness h_{PR}, θ_{PR} is calculated by geometry as

$$\theta_{PR} = \tan^{-1}\left(\frac{h_{PR}}{l_{PR}}\right) = \tan^{-1}\left(\frac{\Delta P}{\Delta l} \cdot \frac{h_{PR}}{P_{res} - P_{th}}\right), \qquad (1)$$

where Δl and ΔP are a length of a moving step and an exposure power, respectively. Considering the selectivity of

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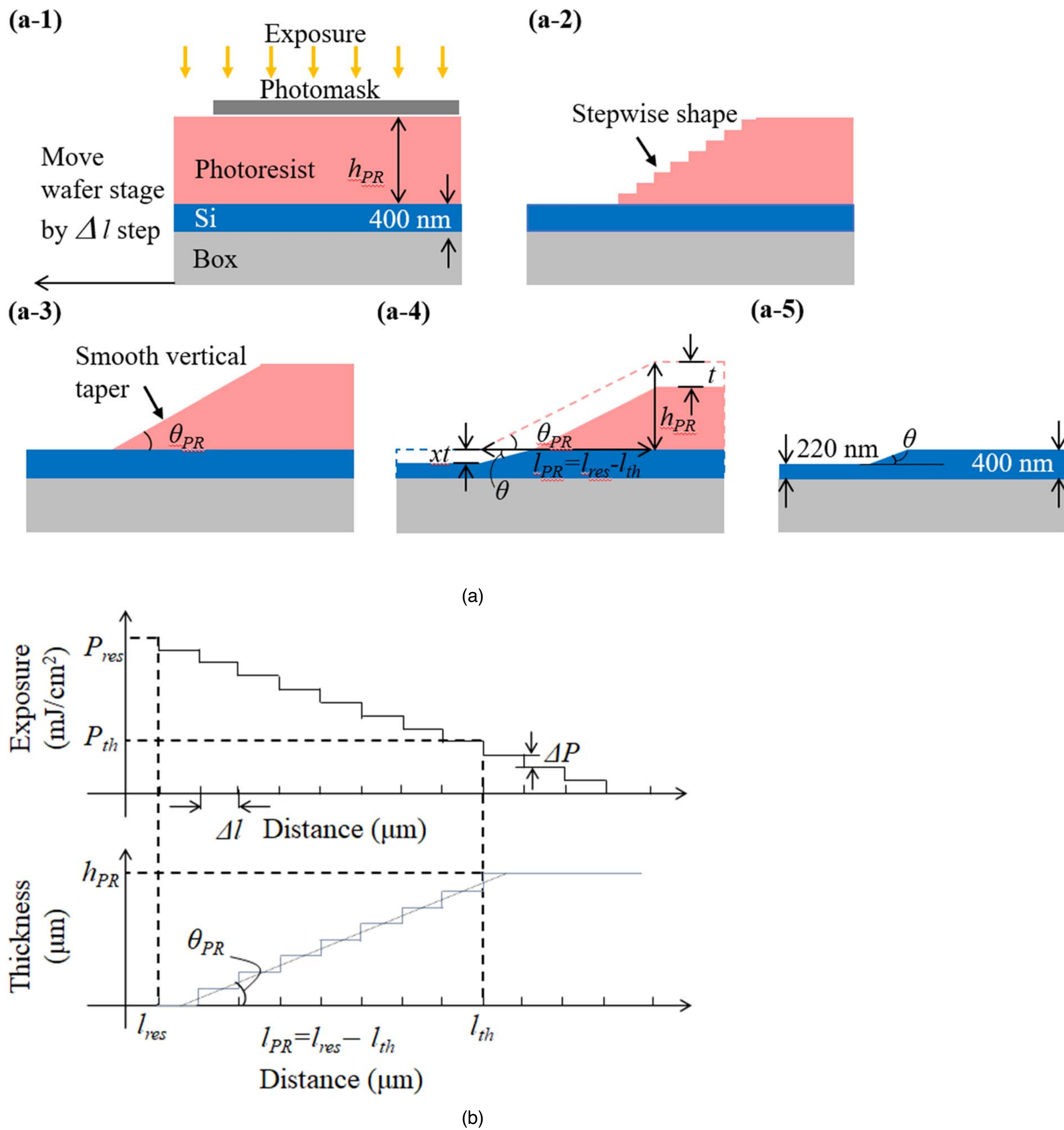

Fig. 3. (Colour online) (a) Process flow of the step-and-exposure lithography. (a-1) Step and exposure by using a commercial stepper. (a-2) Development of the photoresist. (a-3) Photoresist smoothing by baking resist. (a-4) Dry etching of the silicon. (a-4) Fabricated vertical taper structure after photoresist removal. (b) Total amount of exposure and the thickness of the photoresist after development with stepping distance.

etching (x) among photoresist and silicon in Fig. 3(a-4), θ is expressed as

$$\theta = \tan^{-1}\left(\frac{\Delta P}{\Delta l} \cdot \frac{x h_{\mathrm{PR}}}{P_{\mathrm{res}} - P_{\mathrm{th}}}\right). \quad (2)$$

As x is a ratio of etching rates of silicon and photoresist, x depends on the etching condition. As Δl and ΔP are the parameters that can be set on the stepper, Eq. (2) indicates various angles can be fabricated with a single photomask.

4. Fabrication and characterization of vertical tapers

We used an SOI wafer with a 400 nm thick top silicon layer and a 3 μm buried oxide layer. Resin-based positive photoresist, whose thickness (h_{PR}) was 1.7 μm, was used for step-and-exposure lithography. Figure 4(a) shows the photoresist pattern after the development. As can be seen in Fig. 4(a), the thickness of the photoresist gradually changes. After the patterning of the vertical taper structure, silicon was etched to 220 nm by inductively coupled plasma (ICP) with CF_4 and SF_6-based reactive-ion etching (RIE). Then, silicon waveguides were fabricated by electron beam lithography and subsequent ICP-RIE. Figures 4(b) and 4(c) represent a scanning electron micrograph (SEM) and atomic force microscopic image (AFM) of the fabricated vertical-taper waveguide. The smooth vertical taper structure was observed. From the thickness profile of the fabricated Si taper along the waveguide [Fig. 4(c)], the roughness average (RA) of the taper was estimated to be 1.9 nm. Scattering loss caused by the taper roughness can be negligible considering the taper length of 2.4 μm. RA of the etched waveguide was 0.023 nm, which was as smooth as that of the unetched 400 nm waveguide (0.024 nm). The angle of the taper was as low

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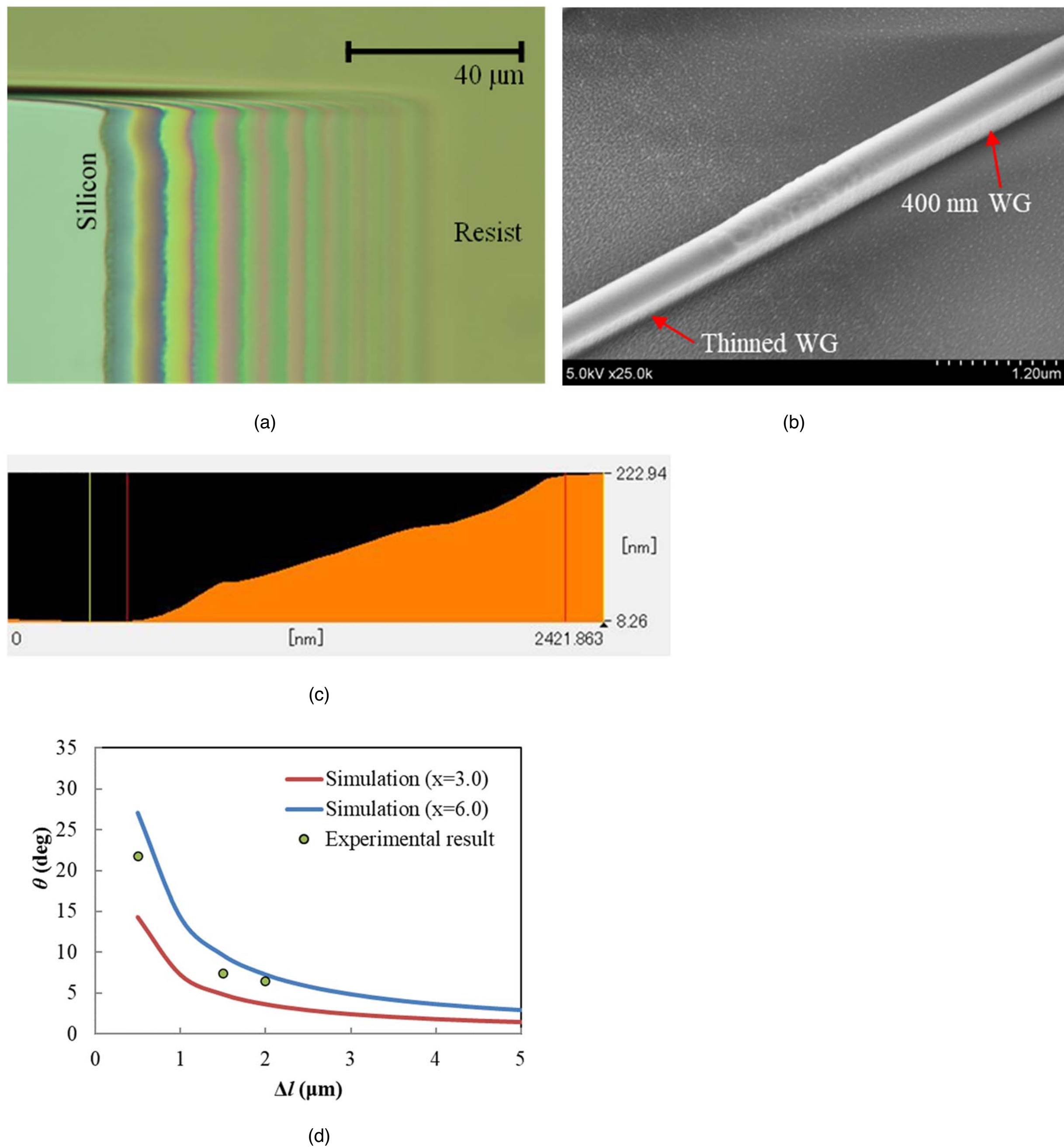

Fig. 4. (Colour online) Microscopic images on each process. (a) Optical microscopic image of the photoresist after development. (b) SEM image and (c) AFM image of the vertical taper. The roughness average of the taper was as low as 1.9 nm. (d) Simulated θ calculated by Eq. (2), where $x = 3$ and 6. Experimental results are also plotted.

as 6.4 degrees. Figure 4(d) shows the simulated angles of vertical tapers calculated from Eq. (2), where ΔP was set to 2 mJ cm^{-2}, P_{th} and P_{res} were experimentally measured to be 18 and 100 mJ cm^{-2}, respectively. x was derived as 3.0–6.0 from the experiment. As can be seen in Fig. 3, the experimental result of θ was consistent with that of the simulation and θ was controlled by Δl, which can be arbitrarily varied by the stepper.

Let us discuss the controllability of the angle. In the ideal case, the roughness of the stepwise shape of the photoresist in Fig. 3(b) can be negligible when ΔP and Δl are set small enough. However, in practice, the minimum value of ΔP and Δl are limited by the equipment, which are 2 mJ and 100 nm in our stepper. When ΔP and Δl are large, the stepwise shape cannot be smoothed completely by the post-baking process, which results in the roughness of the taper. Thus, from Eq. (2), fabricating the extremely larger or smaller angles has a trade-off with the taper roughness. Namely, fabrication of larger angles can be realized by setting smaller Δl at minimum ΔP for smoothness. However, when Δl reaches its minimum value, ΔP should be increased to realize further larger angles, which causes the roughness. Similarly, fabrication of further smaller angles, Δl should be increased at minimum ΔP with the cost of larger roughness. For example, when $\Delta l = 5$ μm to realize the taper for the angles of 2.9°, the RA of the taper became 4 nm, which is twice as much as that of $\Delta l = 2$ μm. The range of angles maintaining the roughness of less than 2 nm is roughly estimated from 6.4° to 60.2°. It is noted that the range of angles or smoothness can be enhanced by optimizing the process, such as by making

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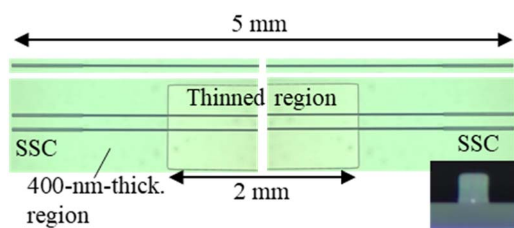

Fig. 5. (Colour online) Fabricated waveguides with and without vertical tapers. The inset shows the cross-section of the SSC. The length of the thinned waveguides was 2 mm.

the selectivity x lower. Optimizing the temperature of post-baking can also enhance the smoothness of photoresists. The photoresist we used was smoothed from the post-baking temperature of 110 °C and no further change up to 130 °C. Exceeding 140 °C resulted in a degradation of the photoresist, and we adapted 120 °C for the post-baking. The angle was not affected by the process and was robust to the post-baking temperature.

After the fabrication of the waveguide, spot-size converters (SSC) were formed on both edges of the waveguide to couple the lensed fibers efficiently. The SSCs are inversed-taper type,[33] second core of which were formed by a photosensitive polymer. Figure 5 represents the optical microscopic image of the fabricated chip, where the upper waveguide is 400 nm in thickness, the rest of the two waveguides have vertical tapers and the 220 nm thick region with 2 mm in length. The width of the waveguides was measured to be 408 nm. The transmission loss was measured for quasi-TE mode at 1310 nm. While the insertion loss of the 400 nm thick waveguide was 6.5 dB, that of the waveguide with vertical tapers was 7.0 dB. The estimated insertion loss of the taper was less than 0.3 dB, which was consistent with the simulation.

5. Conclusions

We have developed a simple fabrication method of silicon vertical-taper structures using step-and-exposure lithography. Also, we have made a model of the lithography and found the angle of the taper can be controlled by the stepper. The simulation was in good agreement with the fabricated taper angle, which indicates the angles can be predicted by using some experimental parameters. Fabricated tapers convert the 400 nm thick SOI silicon waveguide to 220 nm with low-loss. The technology can realize seamless tuning of the silicon thickness and integration of optimal devices.

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