First Demonstration of 25-nm Quad Interface p-MTJ Device With Low Resistance-Area Product MgO and Ten Years Retention for High Reliable STT-MRAM

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***Abstract*—We successfully developed 25-nm quad CoFeB/MgO-interfaces perpendicular magnetic tunnel junction (quad-MTJ) with enough thermal stability. To fabricate the quad-MTJ, a physical vapor deposition (PVD) process for depositing novel free layer and low resistance-area (*RA*) product MgO layer and low-damage fabrication processes were developed. The developed quad-MTJ technology and advanced process bring better tunnel magneto resistance (TMR) ratio and *RA* to quad-MTJ than those of double-interface MTJ (double-MTJ), even though quad-MTJ has an additional MgO layer. Scaling down the MTJ size to 25 nm, we demonstrated the advantages of quad-MTJ compared with double-MTJ as follows: 1) two times larger thermal stability factor (Δ), which results in over ten years retention; 2) superiority of large Δ in the measuring temperature range up to 200 °C; 3) ~1.5 times higher write efficiency; 4) lower write current at short write pulse regions at less than 100 ns; and e) excellent endurance of over 10^{11} thanks to higher write efficiency, which results from the reduced voltage owing to low *RA* and the low damage integration process technology. As a result, the developed quad-MTJ technologies will open the way for the realization of high-density STT-MRAM with low power, high speed, high reliability, and excellent scalability down to 2× nm node.**

***Index Terms*—Interfacial anisotropy type magnetic tunnel junction (MTJ), low resistance-area (*RA*) product MGO, quad interface, spin-transfer-torque magnetoresistive random access memory (STT-MRAM), thermal stability factor.**

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I. Introduction

THE spin-transfer torque [1], [2] magnetic random access memory (STT-MRAM) [3], [4] has been intensively researched and developed by many LSI companies and academic institutions because of its promising candidature as a low-power, high-performance memory in IoT, edge-AI, automobile applications [5], [6]. With the use of CoFeB/MgO-interface perpendicular magnetic tunneling junctions (p-MTJs) [7], the industrial application of STT-MRAM rapidly progressed [8]–[15], and major LSI companies started the mass production of STT-MRAM. However, for further expansion and promotion of its application areas and market, STT-MRAM must be further scaled. Although the double CoFeB/MgO-interface MTJ (double-MTJ) has become the *de facto* standard in current STT-MRAM technology [16], scaling issues still exist because a large enough thermal stability for nonvolatile memory was not obtained in the MTJ size of less than 30 nm.

To overcome this issue, we proposed a quad CoFeB/MgO-interface MTJ (quad-MTJ) structure [17], [18] and demonstrated its performance down to 33 nm [19]. Although the quad-MTJ has some scaling merits over the conventional double-MTJ [20], [21], its performance down to 2× nm has

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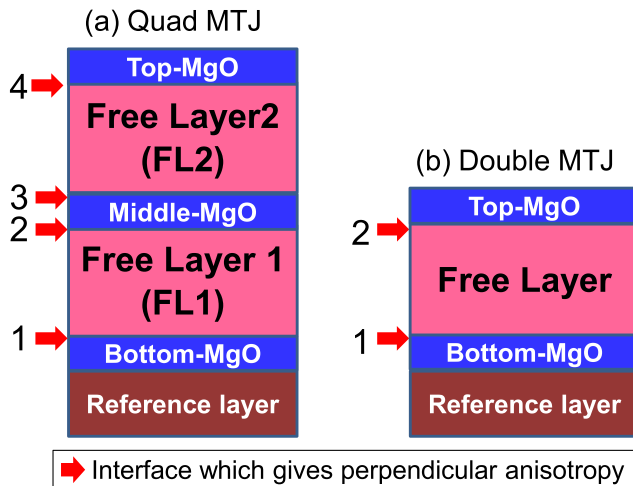

Fig. 1. Design concept of (a) quad CoFeB/MgO interface MTJ and (b) double CoFeB/MgO-interface MTJ. A larger number of the interface in the quad MTJ enables thicker free layer, resulting in high thermal stability [10].

not yet been demonstrated and its technologies have not yet been developed. Furthermore, the read and write properties with slight temperature dependence have been issues for practical usage. As the MTJ size becomes smaller, the influence of the damage regions at the MTJ side-wall becomes more critical [22]. To maintain the intrinsic performance of the quad-MTJ stack with 2×-nm, a low damage MTJ fabrication process is essential.

For scaling down the MTJ, it must have a high thermal stability factor (Δ), high tunnel magnetoresistance (TMR) ratio, and low resistance, simultaneously. Fig. 1 depicts the design concept of quad- and double-MTJs [20]. Quad-MTJ comprises four CoFeB/MgO interfaces; this is twice the number of those in a conventional double-MTJ. This enables a thicker free layer because perpendicular anisotropy originates from the interface. Free Layer1 (FL1) and Free Layer2 (FL2) are ferromagnetically coupled through the middle MgO to increase the effective free layer volume, thus increase the thermal stability of the free layer. Materials of FL 1 and FL 2 are also important to improve high-temperature properties. Thermal tolerance of 400 °C is also required for CMOS back-end-of-line process compatibility. To satisfy these requirements, we developed the fabrication processes of MgO and free layers for 2×-nm quad-MTJ.

II. Advanced PVD Process for 2×-nm Quad-MTJ

Fig. 2 shows the cross-sectional transmission electron microscopy (TEM) photography of quad-MTJ stack structure. Smooth interfaces of MgO layers were obtained by our advanced physical vapor deposition (PVD) processes. Figs. 3 and 4 show comparisons of transport properties of quad- and double-MTJs in the blanket film. The blanket MTJs were measured by the current-in-plane-tunneling (CIPT) method [23]. The TMR ratio of the developed quad-MTJ improved by over 20% owing to the novel MgO deposition process even in the *RA* range of less than 3 $\Omega\mu m^2$ (Fig. 3). Quad-MTJ achieved a high TMR ratio at a low *RA* (Fig. 4) despite a larger number

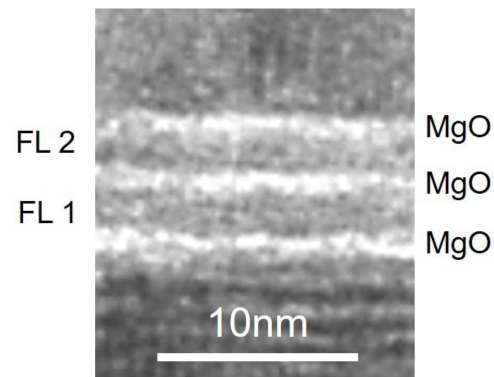

Fig. 2. Cross-sectional TEM photograph of quad-MTJ with advanced PVD process. A clear stack structure with three MgO layers and two free layers is obviously confirmed by our developed PVD process.

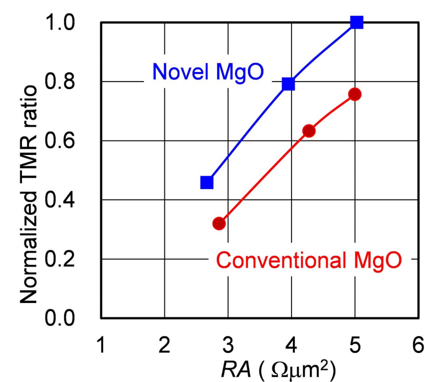

Fig. 3. Improvement of TMR ratio as a function of *RA* for the quad-MTJ in the blanket film. TMR ratio for the quad-MTJ was improved in comparison with quad-MTJ with conventional process owing to novel MgO deposition process.

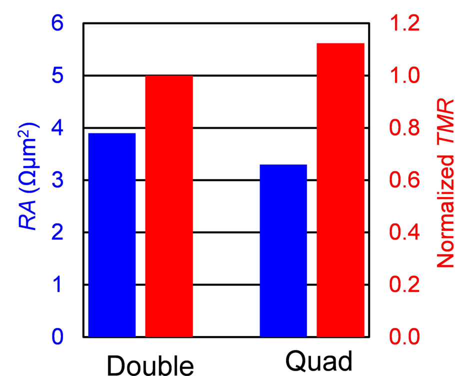

Fig. 4. Improvement of TMR ratio in blanket film by developing the free layers and MgO barrier. Quad-MTJ has a larger TMR ratio at lower *RA* product by free layer material development.

of MgO layers through the development of the free layers and MgO layers. In addition, as a result, a high TMR and a low *RA* were simultaneously realized in the quad-MTJ.

Fig. 5 shows the comparison of temperature (T) dependence of magnetization (magnetic moment per volume: m) for the quad-MTJ normalized by that of the double-MTJ. By a novel free layer development, the quad-MTJ's magnetization normalized by the double-MTJ increases with increasing temperature. This leads to a larger Δ at RT and even larger Δ at high

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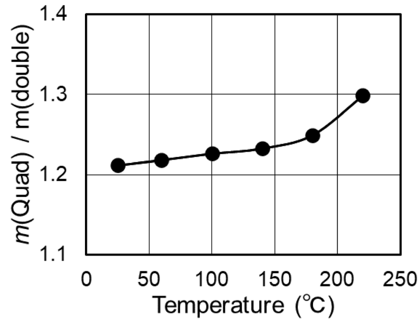

Fig. 5. Comparison of temperature (T) dependence on magnetization (m) of the quad-MTJ normalized by that of the double MTJ. In the quad-MTJ, T dependence of m was improved at higher temperature (∼225 °C) considerably comparing with double-MTJ.

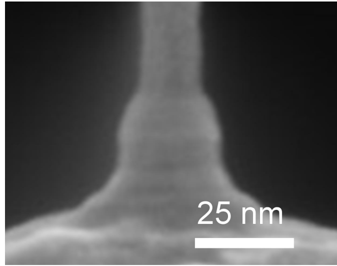

Fig. 6. SEM photograph of 25-nm quad MTJ fabricated through our developed low-damage process. A clear stack structure and etching profile were observed in the MTJ.

temperature in the quad-MTJ compared with the double-MTJ as mentioned later. This is probably due to the temperature dependence of Δ (i.e., magnetic anisotropy) is related to the temperature dependence of magnetization (m).

III. Performances of 25-nm Quad-MTJ

A. Fabrication of 25-nm-Quad-MTJ

By applying the developed advanced process, 25-nm quad-MTJ is successfully fabricated as shown in Fig. 6. The MTJ stacks were deposited using a 300-mm dc/RF magnetron sputtering system and annealed at 400 °C for 1 h after deposition. The stacks were patterned into circular MTJs through electron beam lithography and developed pattern etching process, followed by deposition of the SiN protective layer and electrode wiring.

B. TMR Ratio Dependence on MTJ Size

As shown in Fig. 7, a high TMR ratio of 155% was obtained for the quad-MTJ. Fig. 8 shows the TMR ratio as a function of junction critical dimension (CD) of the quad- and double-MTJs. By developing the novel MgO layer and low-damage process, the TMR ratio of the quad-MTJ was maintained down to 25 nm, which is slightly larger than the double-MTJ for all CD size regions.

C. Δ and I_{C0} Dependence on MTJ Size

Δ and intrinsic critical write current (I_{C0}) were evaluated from the switching probability of the write error rate (WER)

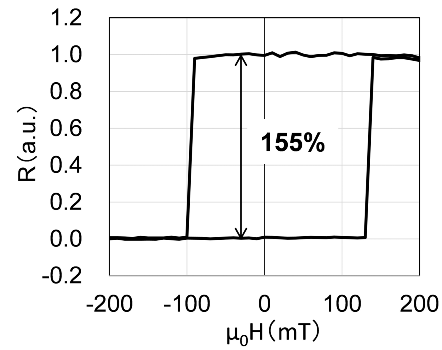

Fig. 7. Typical R–H loop of fabricated 25-nm quad-MTJ. We realized bistable magnetic switching with almost zero-shift magnetic field. TMR ratio shows 155%.

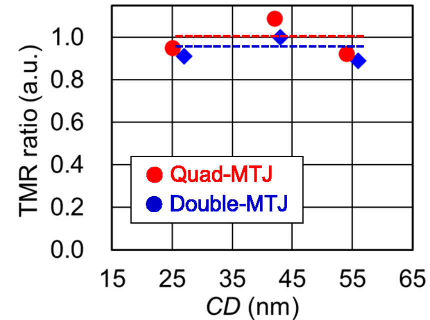

Fig. 8. CD dependence of TMR ratio of the quad- and double-MTJs. TMR ratio of quad-MTJ is almost constant with a decrease in the CD and is slightly larger than those of double-MTJ in all CD ranges.

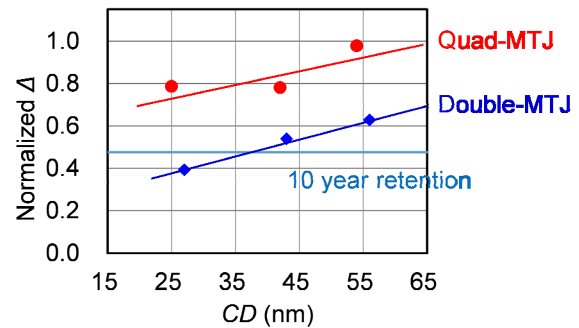

Fig. 9. Normalized thermal stability factor (Δ) at room temperature as a function of junction CD for the quad- and double-MTJs. Δ of the quad-MTJ is almost 1.5–2.0 times larger than that of double-MTJ. Δ of quad-MTJ exceeded those of Ten years' array-data retention ($\Delta = 56$) with 1-ppm error.

with a pulse width of 1 μs. Fig. 9 shows the CD dependence of Δ for the quad- and double-MTJs. By developing the quad-MTJ technology, Δ can be enhanced by a factor of about 1.5–2. Quad-MTJs achieved ten years of retention when CD was down to 25 nm by using a developed low-damage fabrication process. Furthermore, by extrapolating from the measurement results based on the macrospin model, it is expected that ten years of retention will be achieved for the quad-MTJ down to 10 nm. Fig. 10 shows normalized I_{C0} as a function of CD. The I_{C0} was normalized by 55 nm in CD. It was revealed that there is no significant difference in the

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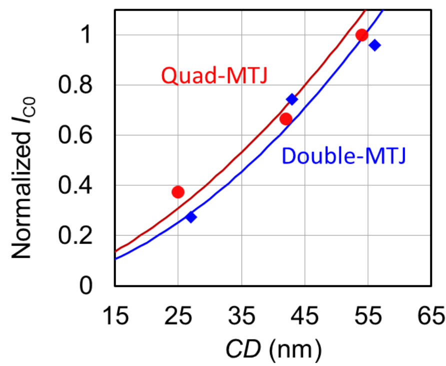

Fig. 10. CD dependence of critical write current (I_{C0}) for the quad- and double-MTJs. The quad-MTJ showed almost same I_{C0} as the double-MTJ in all CD regions.

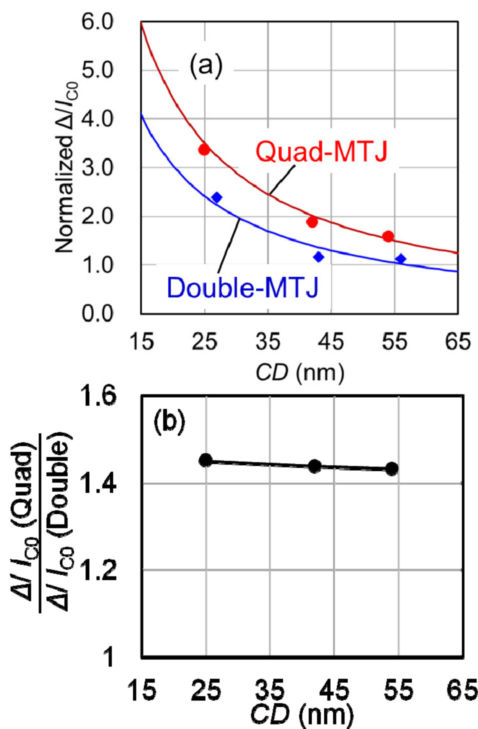

Fig. 11. (a) Write efficiency (Δ/I_{C0}) as a function of junction CD for the quad- and double-MTJs. (b) Δ/I_{C0} of the quad-MTJ was ~1.5 times larger than that of the double-MTJ.

two types of MTJ (quad- and double-MTJs). The relatively weak magnetic coupling between FL1 and FL2 may give a magnetization process that is out of sync with FL1 and FL2 during writing, resulting in a relatively small write current despite maintaining high thermal stability [24], [25]. Therefore, as shown in Fig. 11(a), write efficiency (Δ/I_{C0}) in the quad-MTJs is higher than those of the double-MTJ even in the CD range of 2× nm. The write efficiency (Δ/I_{C0}) in the quad-MTJ and the double-MTJ is about 1.5 in the measured CD range from 2× nm to 5× nm [Fig. 11(b)].

D. Δ Dependence on Temperature

Fig. 12 shows the temperature dependence of the ratio of thermal stability factor for the quad-MTJ and the double-MTJ ($\Delta_{\text{Quad}}/\Delta_{\text{Double}}$). At R.T. (25 °C), Δ of the 25-nm quad-MTJ

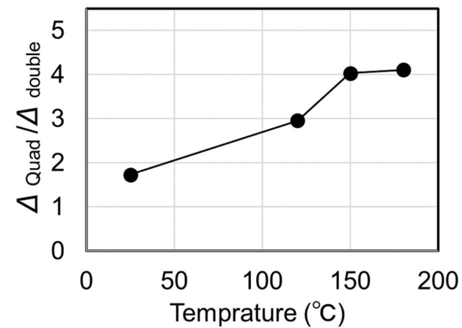

Fig. 12. Temperature dependence of relative thermal stability factor ($\Delta_{\text{Quad}}/\Delta_{\text{Double}}$) in the 25-nm quad-MTJ and the 27-nm double-MTJ. The quad-MTJ showed high performance of thermal stability from 25 °C (R.T.) to 180 °C.

was 1.7 times higher than that of the double-MTJ at almost the same CD and maintains its superiority even when the temperature increases. In addition, the $\Delta_{\text{Quad}}/\Delta_{\text{Double}}$ ratio achieved over 4 at over 150 °C, which means Δ_{Double} decreases much more drastically than Δ_{Quad} with the increase of temperature. That is, quad-MTJ has an advantage even in a high-temperature environment compared to double-MTJ. The reason why the $\Delta_{\text{Quad}}/\Delta_{\text{Double}}$ became larger on the high-temperature side is considered to relate with the improvement of the temperature dependence of m(Quad)/m(Double) as shown in Fig. 5, because Δ is proportional to M_s, and free layer is thicker in quad-MTJ.

E. Write Error Rate

The write voltage dependence of WER was evaluated for the 25-nm quad-MTJ and the 27-nm double-MTJ (Fig. 13). In comparison with the double-MTJ, the quad-MTJ has a sharper WER curve, because the Δ of the quad-MTJ is larger than that of the double-MTJ [19] and a high TMR ratio of quad-MTJ has high spin transfer efficiency. Furthermore, the quad-MTJ has a better slope of the WER shape than the double-MTJ until high-speed writing of 10 ns. The WER was measured down to 10^{-6} with t_w(s) of 10 and 30 ns for the quad MTJ, and it showed that almost no change from the tendency up to 10^{-4} [Fig. 14]. That is, the quad-MTJ can suppress the write voltage at a higher speed write operation compared to the double-MTJ.

F. Switching Field Versus Voltage

Fig. 15 shows the switching field (H_{sw}) dependence of bias voltage (V_b) for the quad-MTJ and the double-MTJ. Fittings were performed with quadratic functions [26]. Coefficients of V^2 are thought to correlate with self-heating effects. Coefficients of V^2 normalized by resistance-area (RA) product for quad-MTJs are nearly the same as those for double-MTJs. These results suggest the self-heating effects of the quad-MTJ are similar to those of the double-MTJs.

G. Write Speed Versus Write Current

Fig. 16 shows the dependence of the write current (I_C) on the write pulse width (t_W) for the 25-nm quad-MTJ and the

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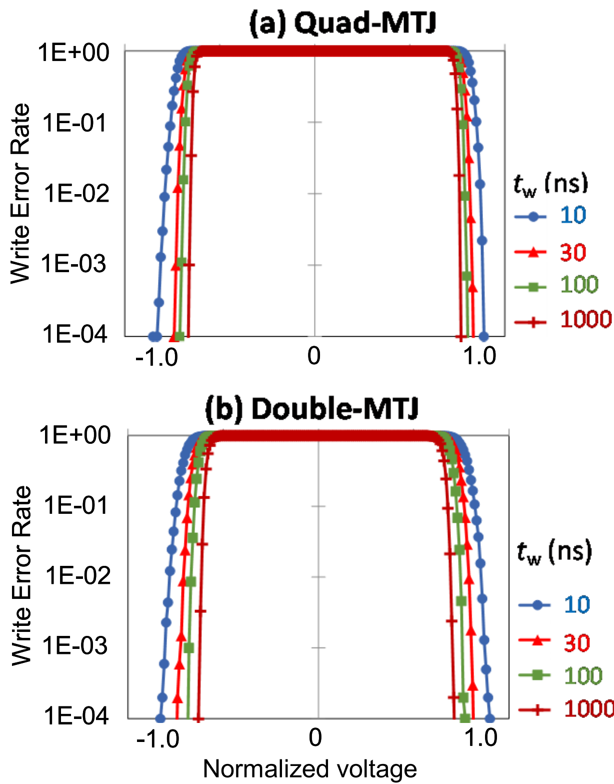

Fig. 13. Write pulse width (t_W) dependence of WER at different write voltage for (a) 25-nm quad-MTJ and (b) 27-nm double-MTJ. The voltage was normalized by double-MTJ with 10 ns. In comparison with the double-MTJ, the quad-MTJ has a sharper WER curve.

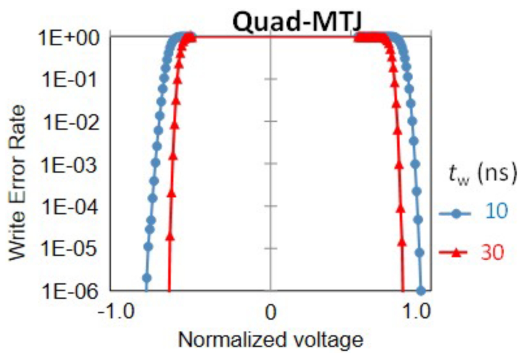

Fig. 14. WER down to 10^{-6} for high speed switching at different write voltage (V) for the 34-nm quad-MTJ.

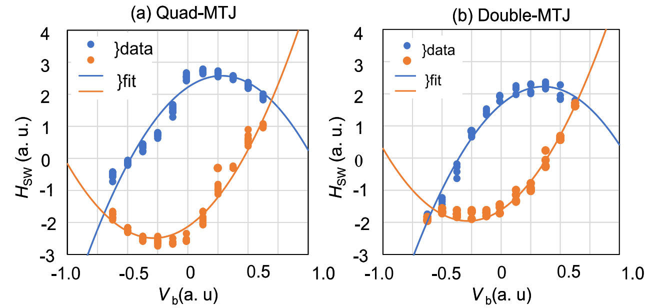

Fig. 15. H_{SW} versus V_b data for (a) quad-MTJ and (b) double-MTJ. Fitting was performed with quadratic functions [26].

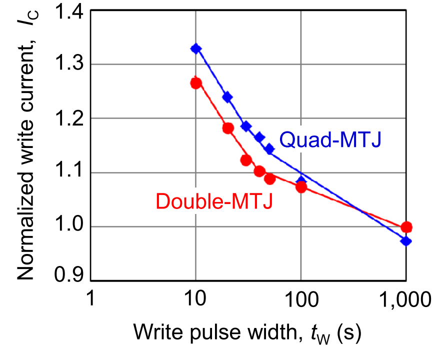

Fig. 16. Dependence of the write current (I_C) on the write pulse width (t_W) for the 25-nm quad-MTJ and the 27-nm double-MTJ. Although the quad-MTJ has high Δ, I_C of quad-MTJ can be decreased at $t_W < 100$ ns that is real usage condition, compared to that of the double-MTJ.

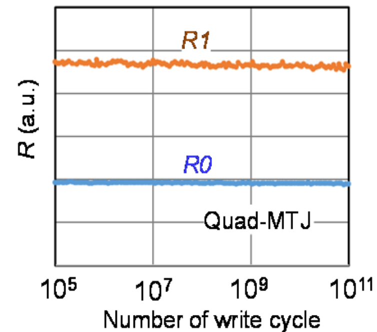

Fig. 17. Endurance result of the 25-nm quad-MTJ. Although the quad-MTJ enhances Δ by a factor of ~2, its endurance exceeds that of a conventional MTJ by at least 10^{11}.

27-nm double-MTJ. I_C of the quad-MTJ shows a larger value than that of the double-MTJ at t_W of 1 μs. In contrast, I_C of the quad-MTJ shows a smaller value than that of the double-MTJ in a shorter write pules range ($t_W < 100$ ns), which is a real usage condition. These advantages of 25-nm quad-MTJ are realized by the less sensitiveness against thermal excitation in the case of MTJ with higher Δ [10].

H. Endurance

Fig. 17 shows the endurance performance of the 25-nm quad-MTJ; it achieves an endurance of over 10^{11}, while maintaining over ten years retention owing to its higher write efficiency than that of the double-MTJ with low *RA*.

IV. Conclusion

We successfully demonstrated a thermally stable quad-MTJ down to 25 nm. As presented in Table I, by developed quad-MTJ technology and low damage fabrication processes, our 25-nm quad-MTJ has a low *RA* of 3 $\Omega\mu m^2$, twice Δ of the double-MTJ, high write efficiency, 10-ns high-speed writing, ten-year retention, and 10^{11} endurance at the same time. Moreover, by these developed technologies, advantages of the quad-MTJ such as large Δ and high write efficiency are kept even though the quad-MTJ size was scaled down from

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TABLE I

SUMMARY OF THE DEVELOPED QUAD-MTJ TECHNOLOGY OVER THE DOUBLE-MTJ TECHNOLOGY. THE QUAD-MTJ HAS MORE THAN TEN YEARS OF RETENTION DOWN TO 25 nm, 10^{11} ENDURANCE PERFORMANCE AND LOW *RA* PRODUCT. MOREOVER, ADVANTAGES OF QUAD-MTJ ARE KEPT EVEN THOUGH THE QUAD-MTJ SIZE WAS SCALED DOWN FROM 33 TO 25 nm AND *RA* DECREASED FROM 5 TO 3 $\Omega\mu m^2$

	Developed 25nm Quad-MTJ in this work	Quad-MTJ at VLSI2020 [13]	Double-MTJ at IEDM2018 [4]
Junction CD	25 nm ~ ⬅	33 nm ~	55 nm ~
RA	3 $\Omega\mu m^2$ ⬅	5 $\Omega\mu m^2$	Not disclosed
Thermal stability Δ	Improved by a factor 2 in 25 nm	Improved by a factor 2 in 3X nm	Factor1 for Δ in 5X nm
Write efficiency Δ / I_{c0}	Improved by a factor ~1.5@10 ns	Improved by a factor ~2.2 @10ns	Factor1 for Δ / I_{c0}
Write speed	10 ns @25nm	10 ns @33nm	14 ns
Retention	>10 years @25nm	>10 years @33nm	>10 years @55nm
Endurance	> 10^{11}@25nm	> 10^{11} @33nm	> 10^{10}

33 to 25 nm and *RA* decreased from 5 to 3 $\Omega\mu m^2$. These quad-MTJ technologies will contribute to the further scaling of the 2× nm STT-MRAM and high reliable STT-MRAM applications, such as automobile and factory automation, etc.

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